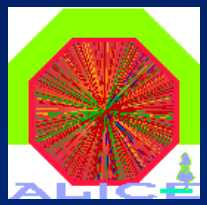
12th Workshop on Electronics for LHC and Future Experiments



The Level 0 Pixel Trigger System for the ALICE experiment

G. Aglieri Rinella[1], A. Kluge[1], M. Krivda[1,2]

On behalf of the SPD project in the ALICE collaboration

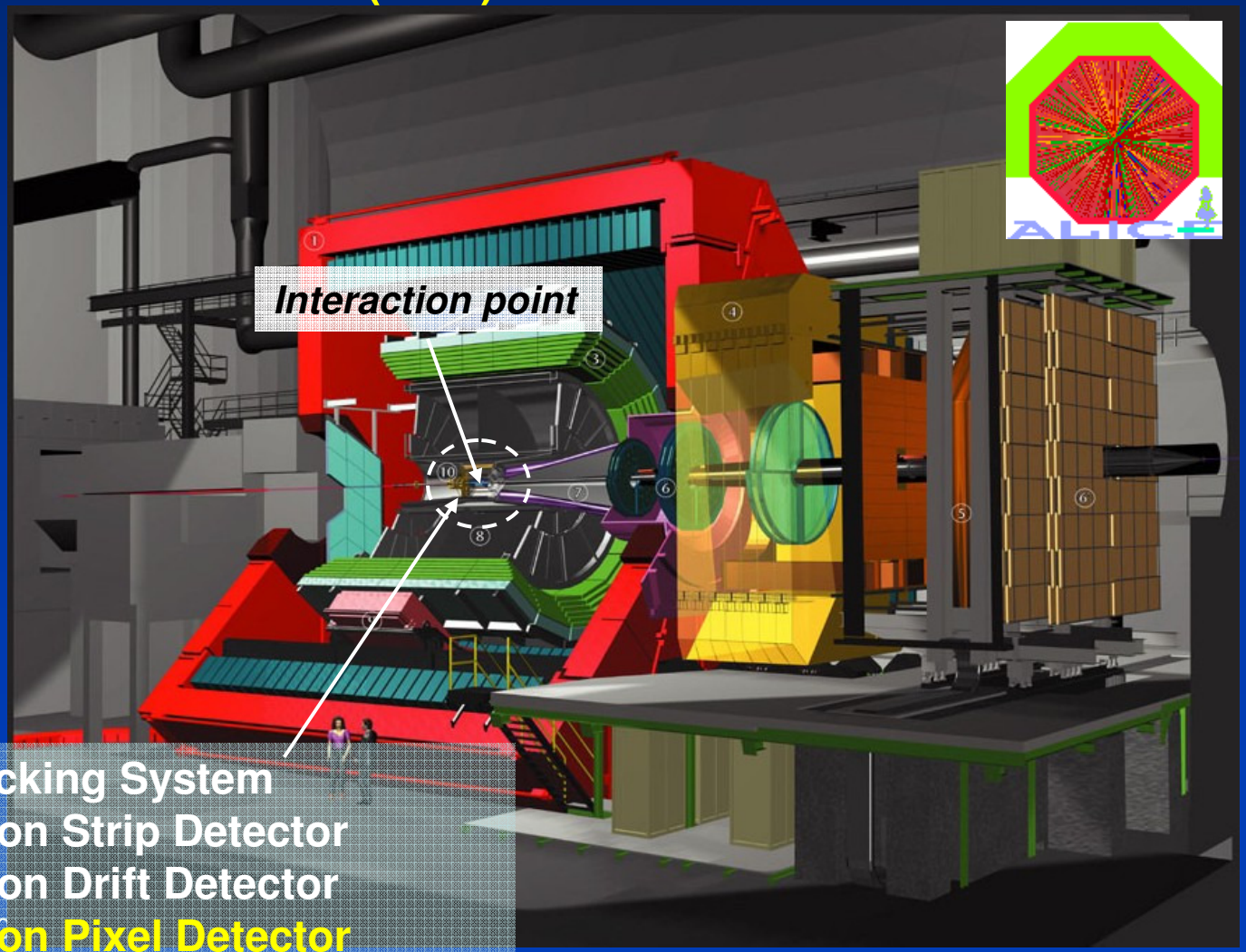
1. **Introduction**
2. **Specifications and constraints**
3. **System design**
4. **Development and testing**
5. **Status of the project**

[1]CERN European Organization for Nuclear Research, Geneva, Switzerland

[2]Institute for Experimental Physics, Kosice, Slovakia

The ALICE experiment

- Nucleus-nucleus collisions at the LHC collider: quark-gluon plasma
- Research program on p-p interactions
- Silicon Pixel Detector (SPD)

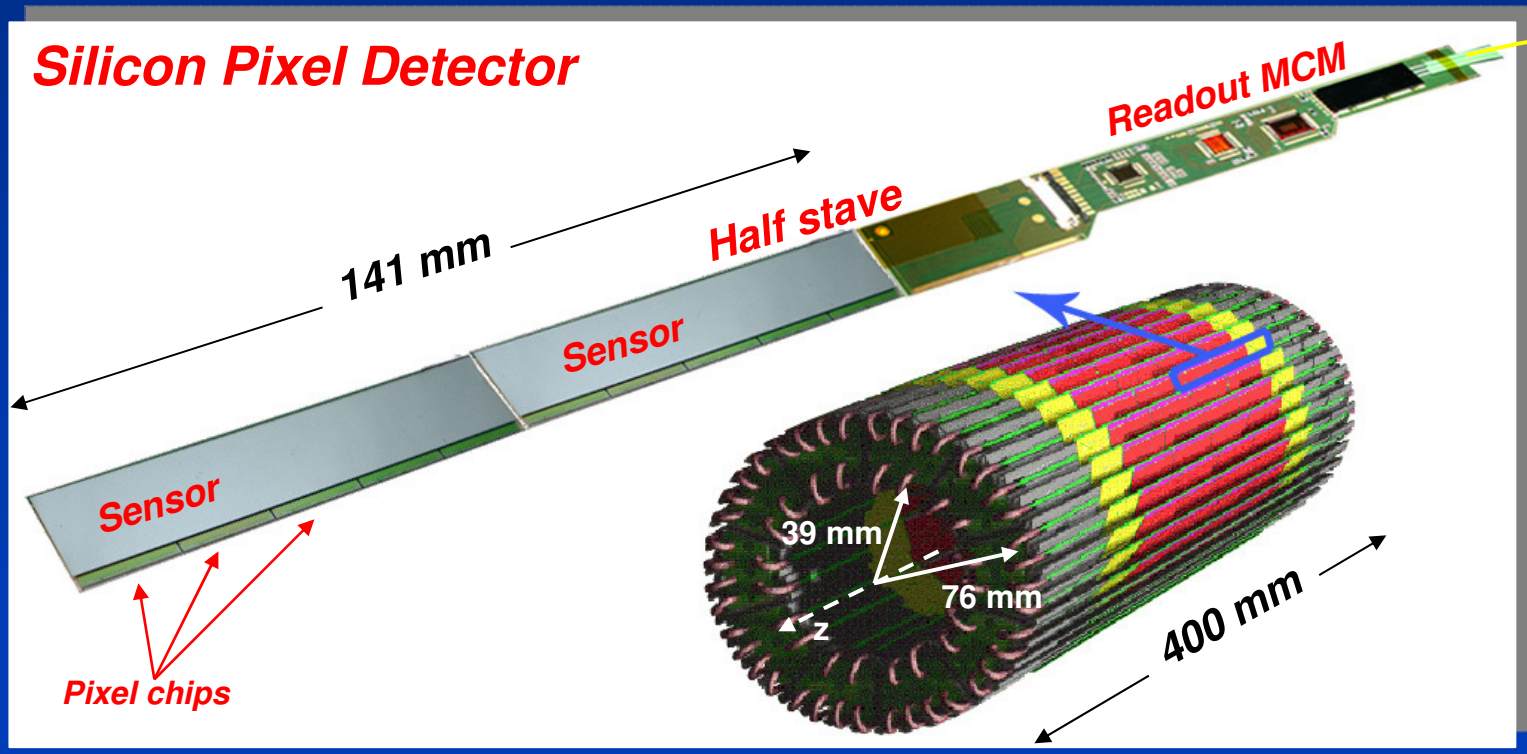


- Inner Tracking System
  - Silicon Strip Detector
  - Silicon Drift Detector
  - Silicon Pixel Detector

Silicon Pixel Detector

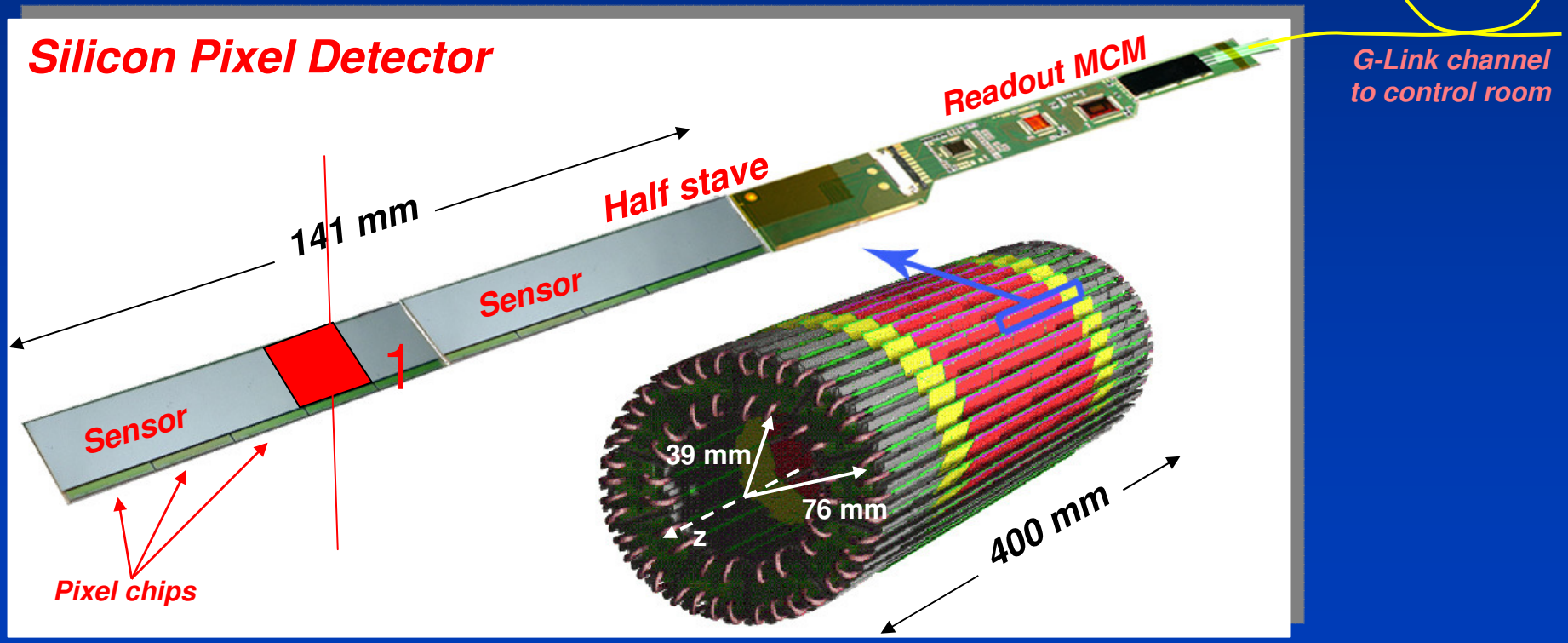
- 120 ***half staves***
  - 2 sensors (160x256 pixels of 425x50 μm^2)
  - 10 readout Pixel chips (32x256=8192 channels)
  - 1 on detector readout Multi Chip Module
  - 1 data output 800 Mb/s 1310 nm digital optical link (G-Link)

More details: oral presentation by M. Krivda, "Alice SPD readout electronics", this conference, this session



Fast-OR

- **Fast-OR signals**
  - **At least 1 pixel hit out of 8192 in a readout chip**
  - **1200 Fast-OR signals, 10 on each of 120 data links**
  - **Low granularity: 1200 equivalent pixels with the size of a chip (~13x13 mm², *pad* detector)**
  - **Transmitted *continuously* every 100 ns**

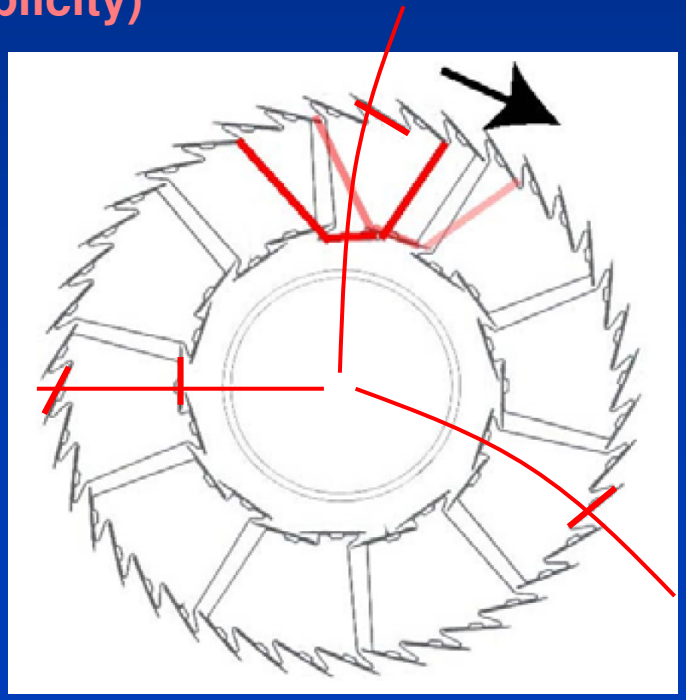


SPD Fast-OR Trigger

- **Use the low granularity (chip level) Fast-OR information as input to the Central Trigger Processor for Level 0 decision**
  - **Multiciplity trigger in p-p collisions (ALICE-INT-2005-25)**
  - **Centrality trigger and selection of impact parameter in heavy ions collisions)**

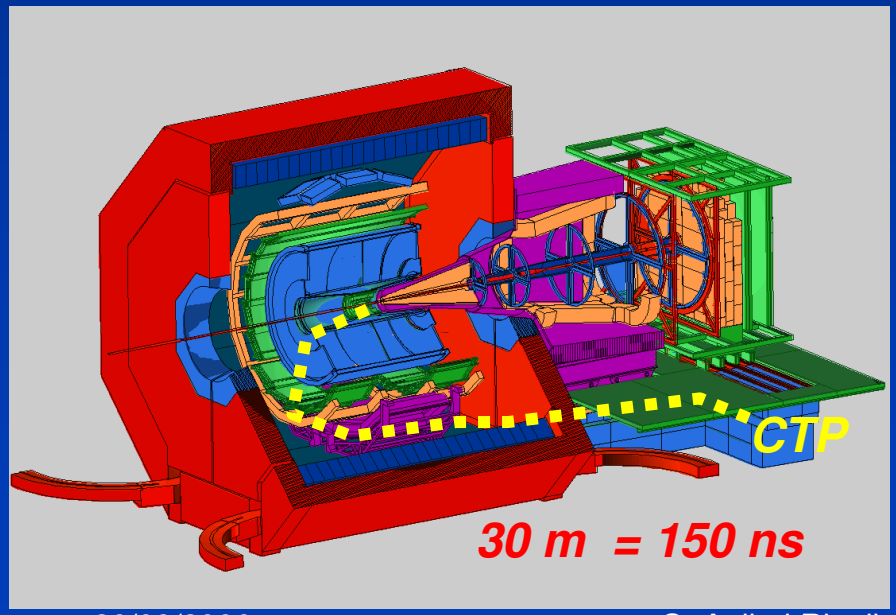
  (J. Conrad, "*Pixel Fast-OR Progress Report*", 28/11/2005)

- **Different algorithms proposed (topology and multiplicity)**
  - **GLOBAL OR**
  - **LAYER**
  - **SECTOR**
  - **HALF SECTOR**
  - **SLIDING WINDOW**
  - **VERTEX**
  - **OCCUPANCY**
- **Combinational functions of 1200 Fast-OR bits**
- **Implementation in *large FPGA***



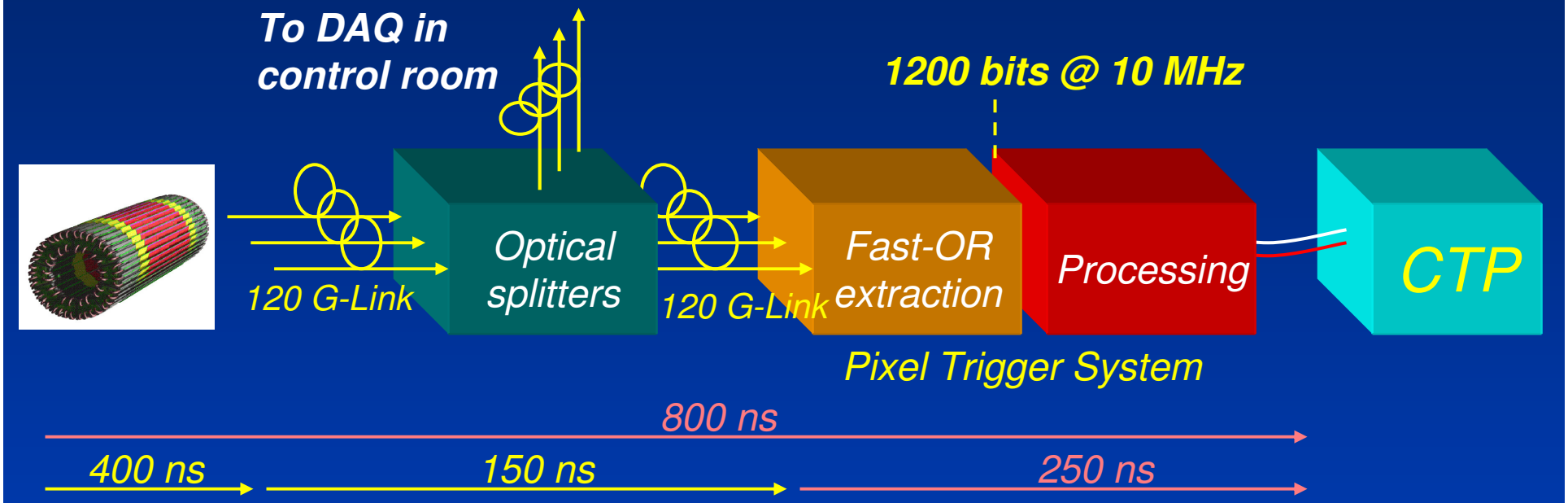
Requirements

- **Requirements**
  - **Extract the 1200 Fast-Or signals from the 120 optical data links**
  - **Process them**
  - **Generate output for the Central Trigger Processor**
  - **Support of various trigger algorithms on the same hardware**
  - **User definable trigger algorithms and remote configuration and control (control room)**



- **Constraints**
  - **Overall process latency: 800 ns (ALICE TDR 010 CERN-LHCC-2003-062)**
  - **No interference on the existing data readout chain**
  - **System location and space occupation**

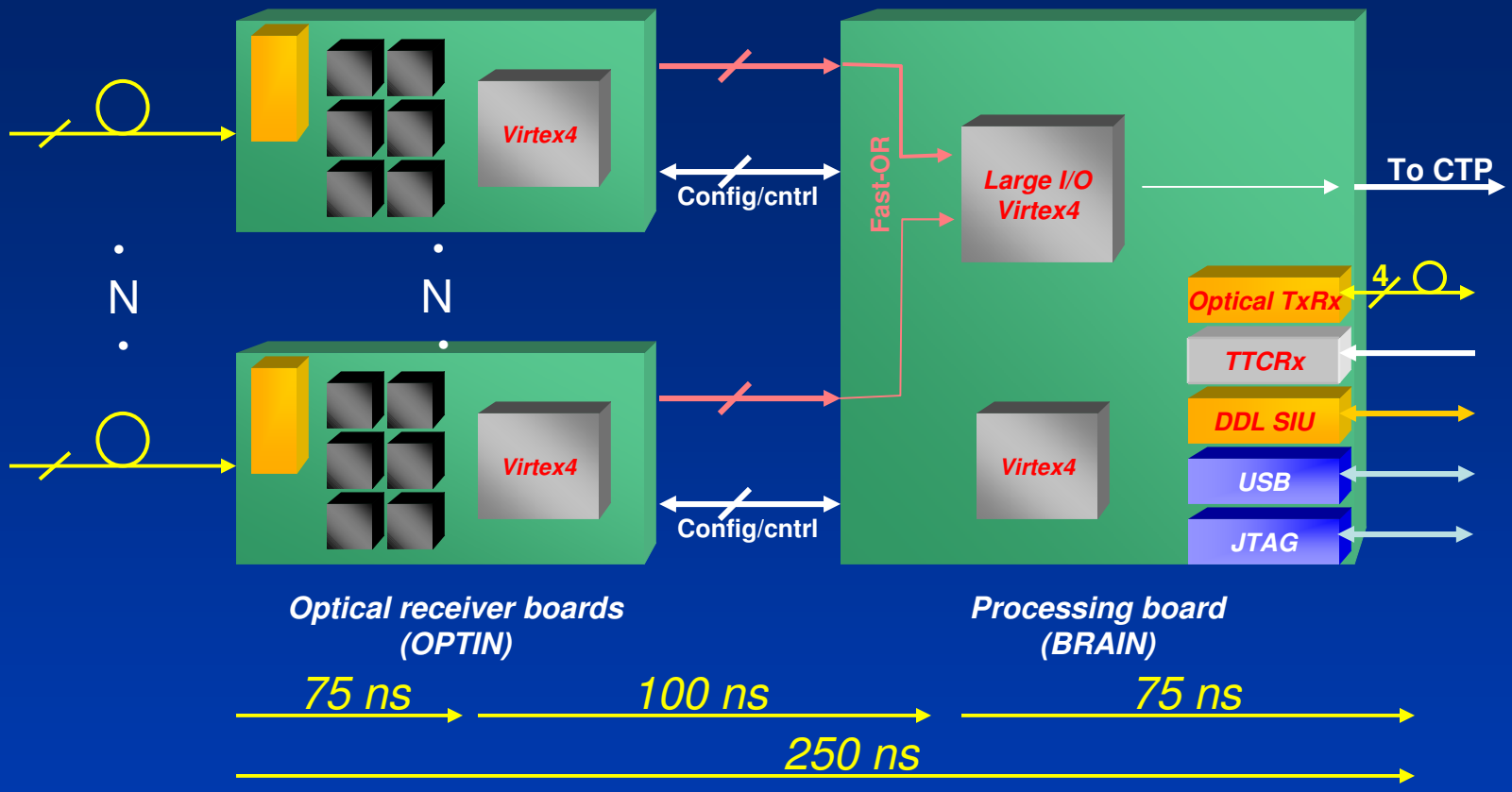
What do we need to build ?



Input bandwidth: 120 • 0.8 Gb/s = 96 Gb/s
(120 • 1.6 Gb/s) = 192 Gb/s

Output bandwidth: 10 Mb/s

System architecture



Large number of simultaneous inputs to the processing FPGA

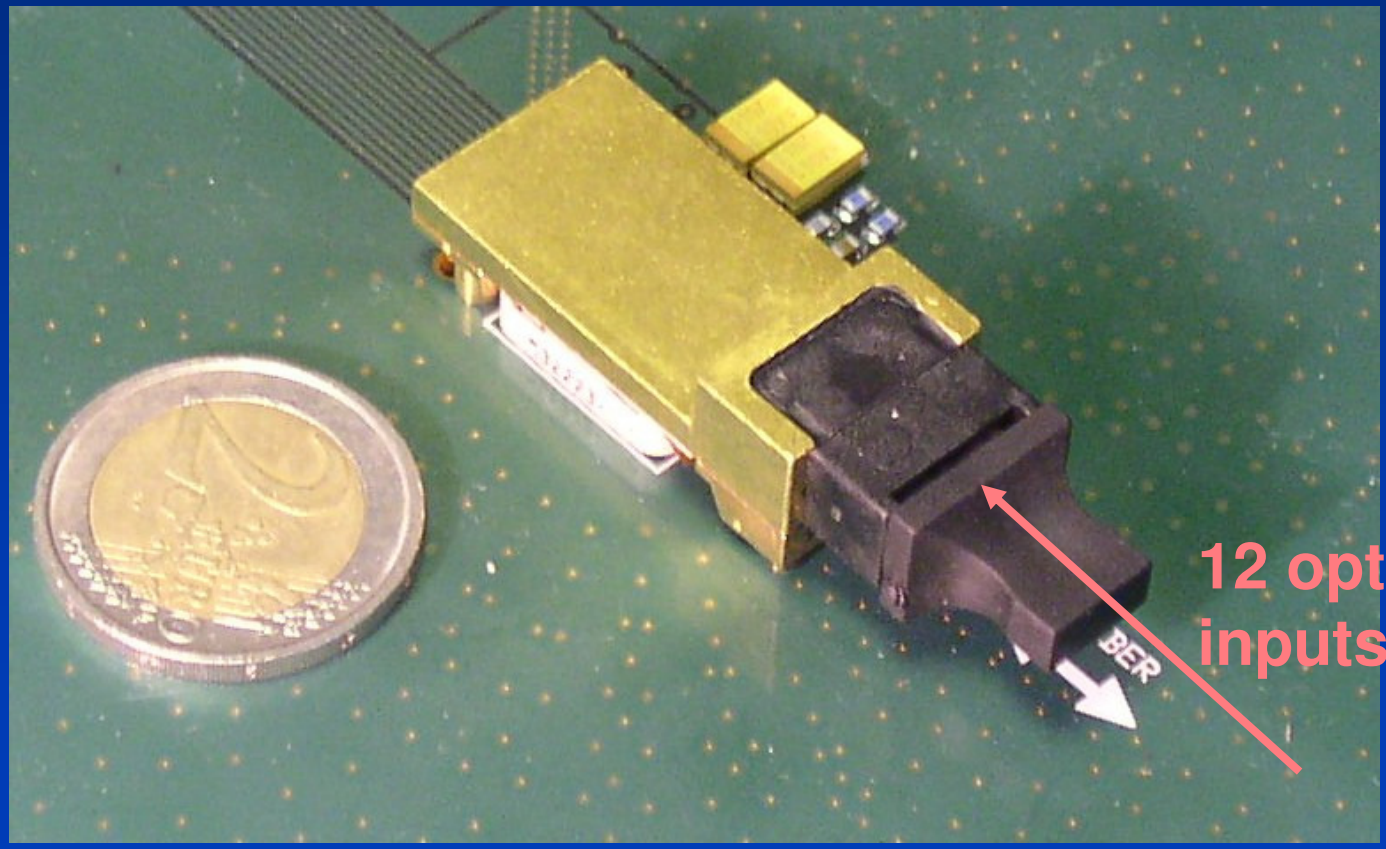
High degree of parallelism: latency constraint

Processing time: < 15 ns

Limiting factor: data deserialization and extraction

Optical receiver modules

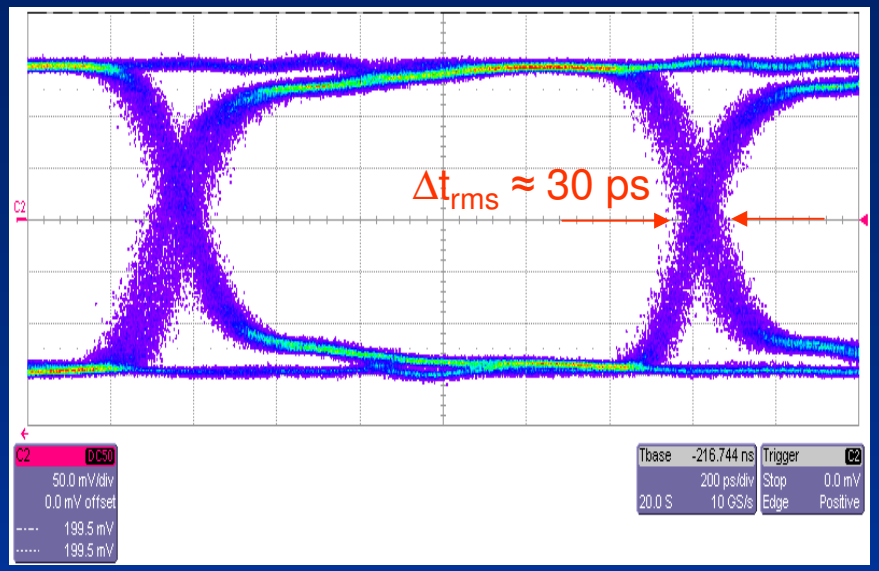
- **Compact** multi channel optical receiver modules @ 1310 nm ***were not found*** off the shelf
- **Zarlink** provided two prototypes of ***12 inputs*** optical fiber receiver modules operating @ 1310 nm
- Significant space saving can be achieved with respect to Small Form Factor standard receivers

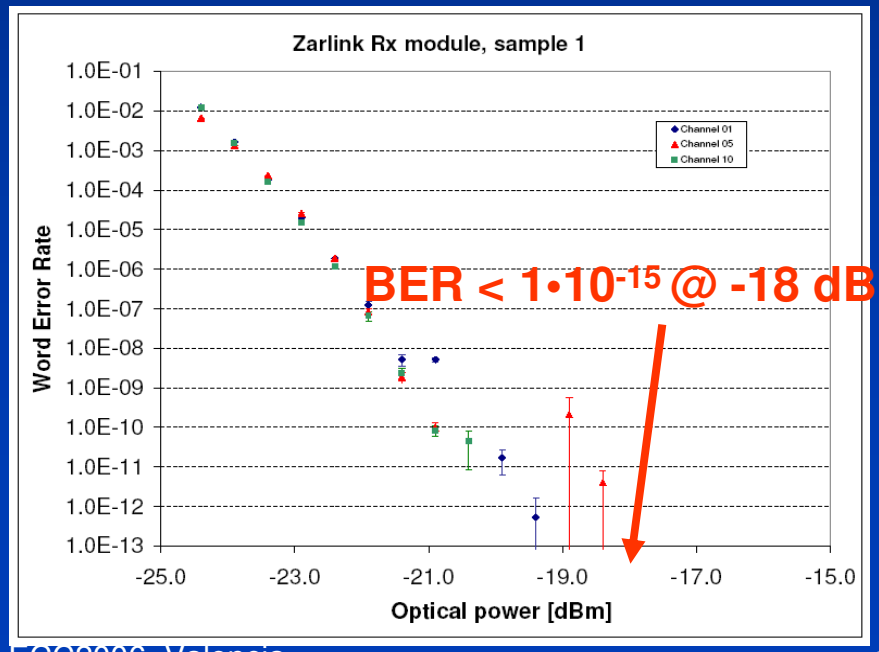


Optical receiver modules (qualifying)

- Experimentally qualified
  - Sensitivity
  - Bandwidth (exceeds requirements)
  - Word Error Rate
- The samples fully satisfied the requirements

- *A set of customized receivers has been ordered*

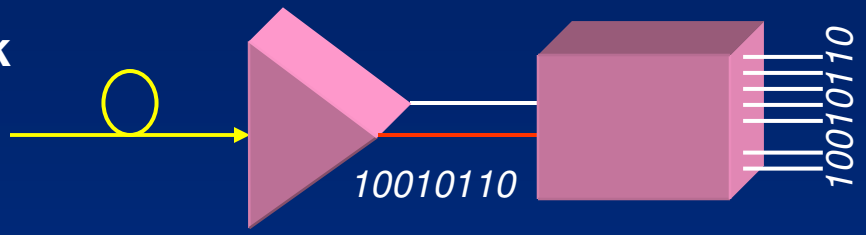


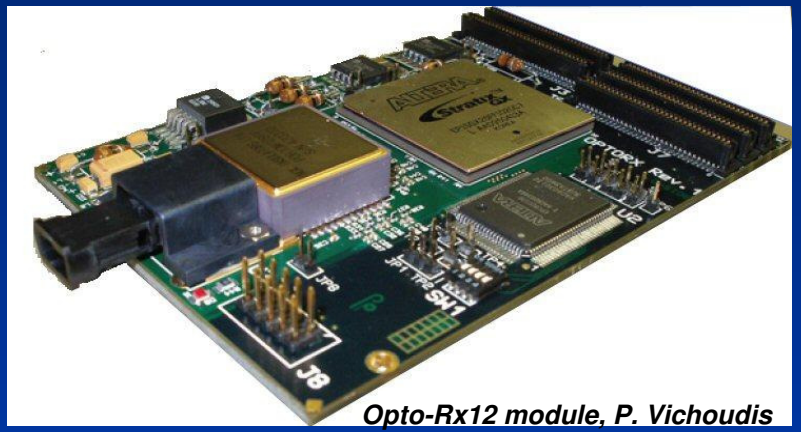


G-Link deserializers

- **Fast-OR bits are the payload of the G-Link serial link control words**
  - Deserialization and frame alignment
- Three solutions:
  - **Altera** Stratix GX
  - **Xilinx** Virtex 2 Rocket I/O
  - **Dedicated ASIC** (Agilent HDMP1034)

- Tested:
  - Altera Stratix GX G-Link deserializer (hardware test)
  - Virtex 2 Rocket I/O deserializer (simulation)





Opto-Rx12 module, P. Vichoudis

S. Reynaud, P. Vichoudis, "A multi-channel optical plug-in module for gigabit data reception", this workshop

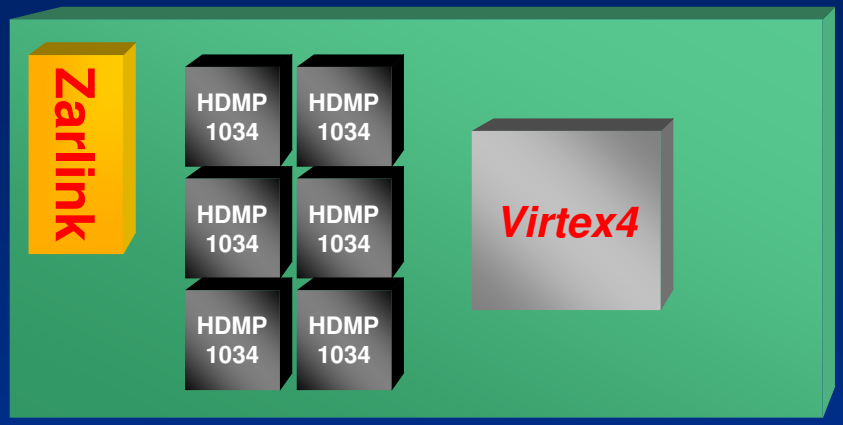
Device	Latency [ns]		
	Data sheet	Simulated	Measured
Agilent HDMP 1034	88	n.a.	87± 7
Altera Stratix (ver1)	n.a.	190	190
Altera Stratix (ver2)	n.a.	130	n.a.
Virtex II Rocket IO X	475	475	n.a.

Realignment and 8B/10B decoding blocks cannot be bypassed !!

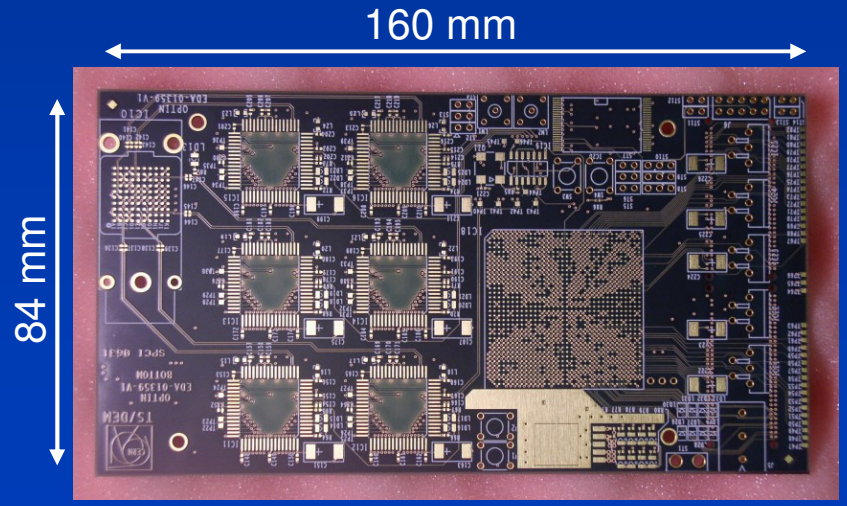
Optical receiver boards - OPTIN

12 optical inputs
1 Zarlink Parallel Fiber Optic Module
12 Agilent HDMP 1034 G-Link deserializers
1 Xilinx Virtex 4 FPGA (Fast-Or extraction)

Serves two half sectors (6+6 half staves)
- Extracts 10 Fast-OR bits from each link
- 120 Fast-OR signals



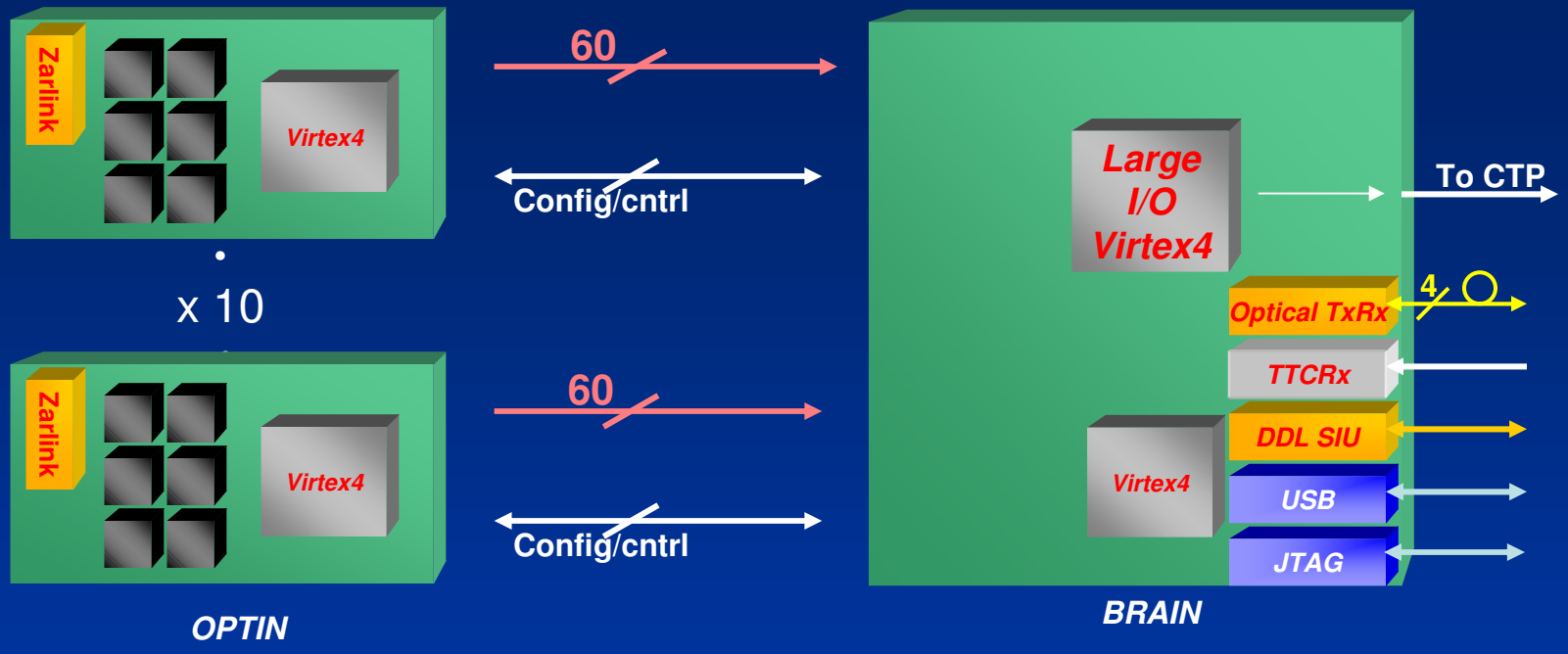
Design and layout
PCB prototype production
Installation of components
Testing
Full firmware implementation
Production



Almost a Compact PCI card !
- Dimensions are larger than the IEEE 1386 envelope

12 layers PCB

Signal routing

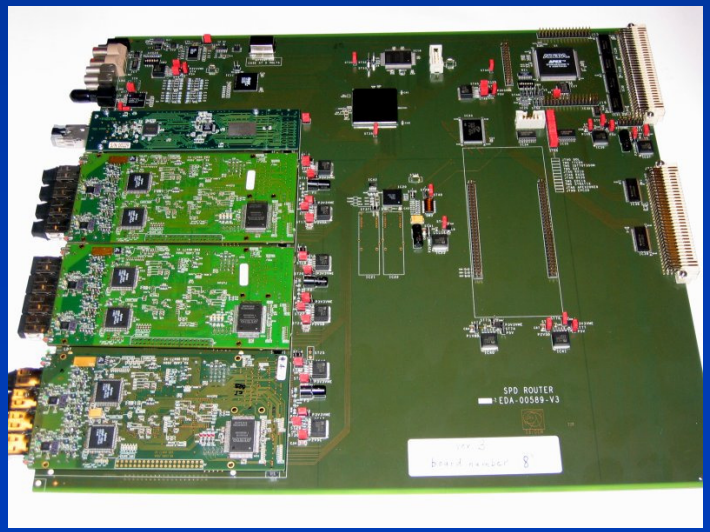


Interconnections and routing between OPTIN and BRAIN

- **Backplane**
- **Flat cables**
- **Daughter cards**

Time division multiplexing on 60 lines per OPTIN

Experience with the Router and LinkRx cards of the data readout system (M. Krivda, SPD readout electronics)



Processing Board – BRAIN

9U motherboard

Large I/O space FPGA, 1500 pins

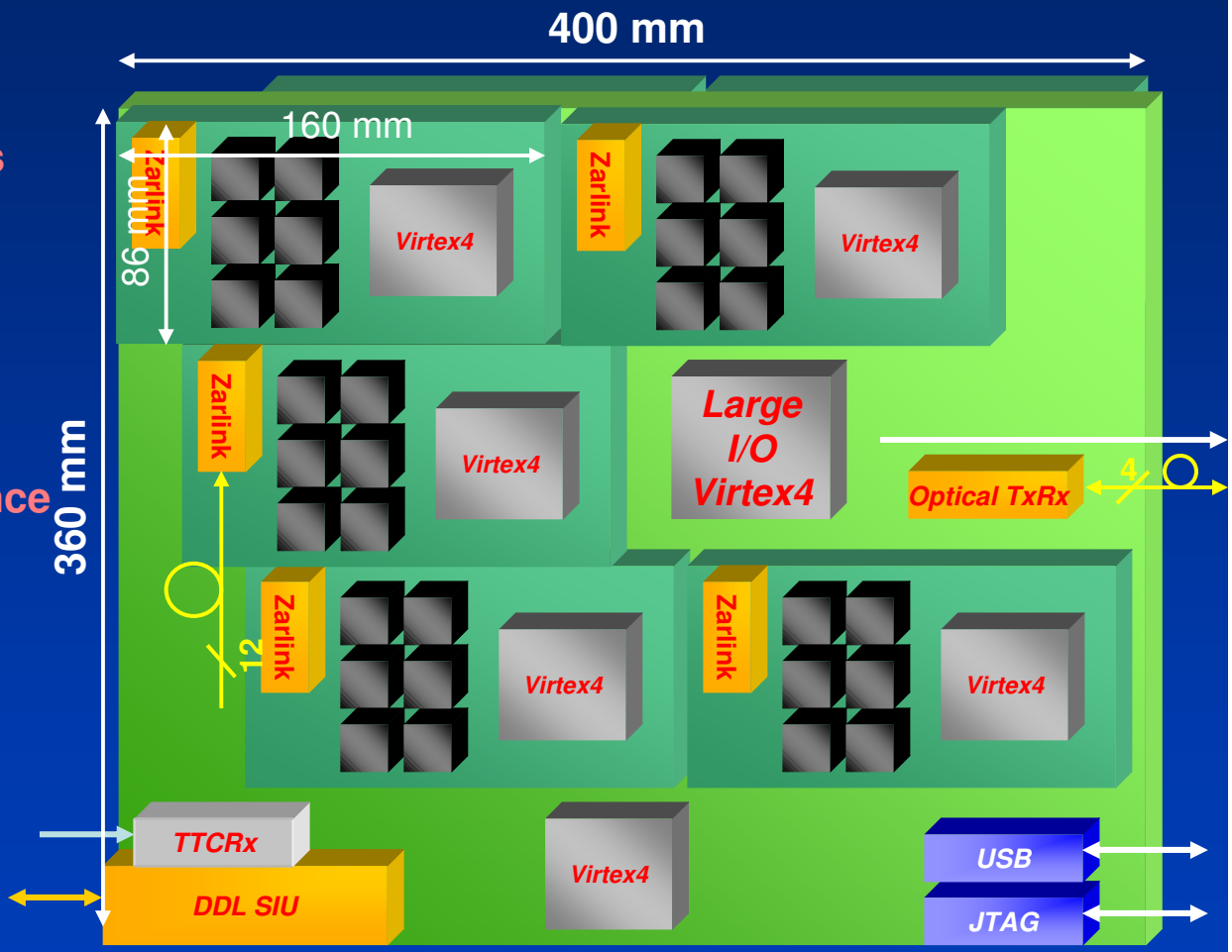
5 OPTIN boards on each side as mezzanine cards

Routing of ~ 1000 lines in the motherboard

- 800 point to point impedance matched single ended lines
- Digitally Controlled Impedance

Auxiliary high speed (400 Mbps) optical or LVDS I/O channels

Layout ongoing



Monitoring, control and configuration

Status monitoring and control via Alice Detector Data Link (DDL)

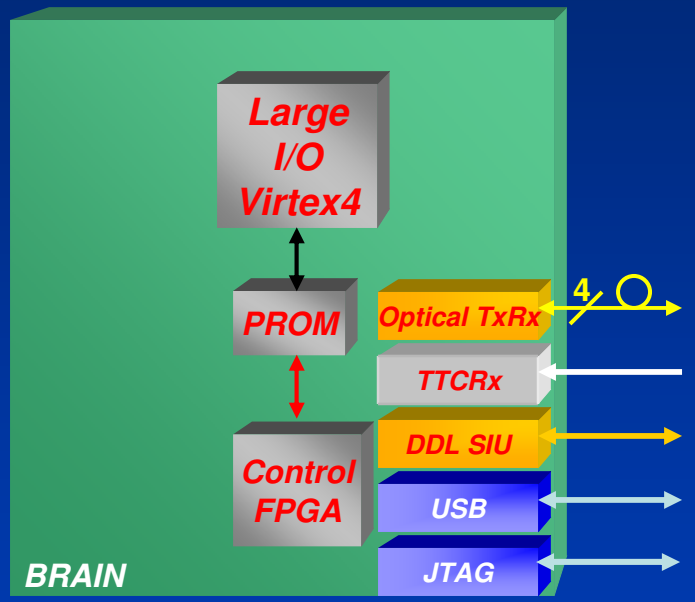
- Control FPGA
- Status and control registers in each FPGA

Remote hardware reconfiguration (via DDL) to change the processing algorithm

- Download firmware in local SRAM memory
- Program PROMs via JTAG players
- Launch FPGA reconfiguration

Debugging and local access interfaces (USB, JTAG)

Integration of the system in the Alice Detector Control System



Power dissipation and cooling

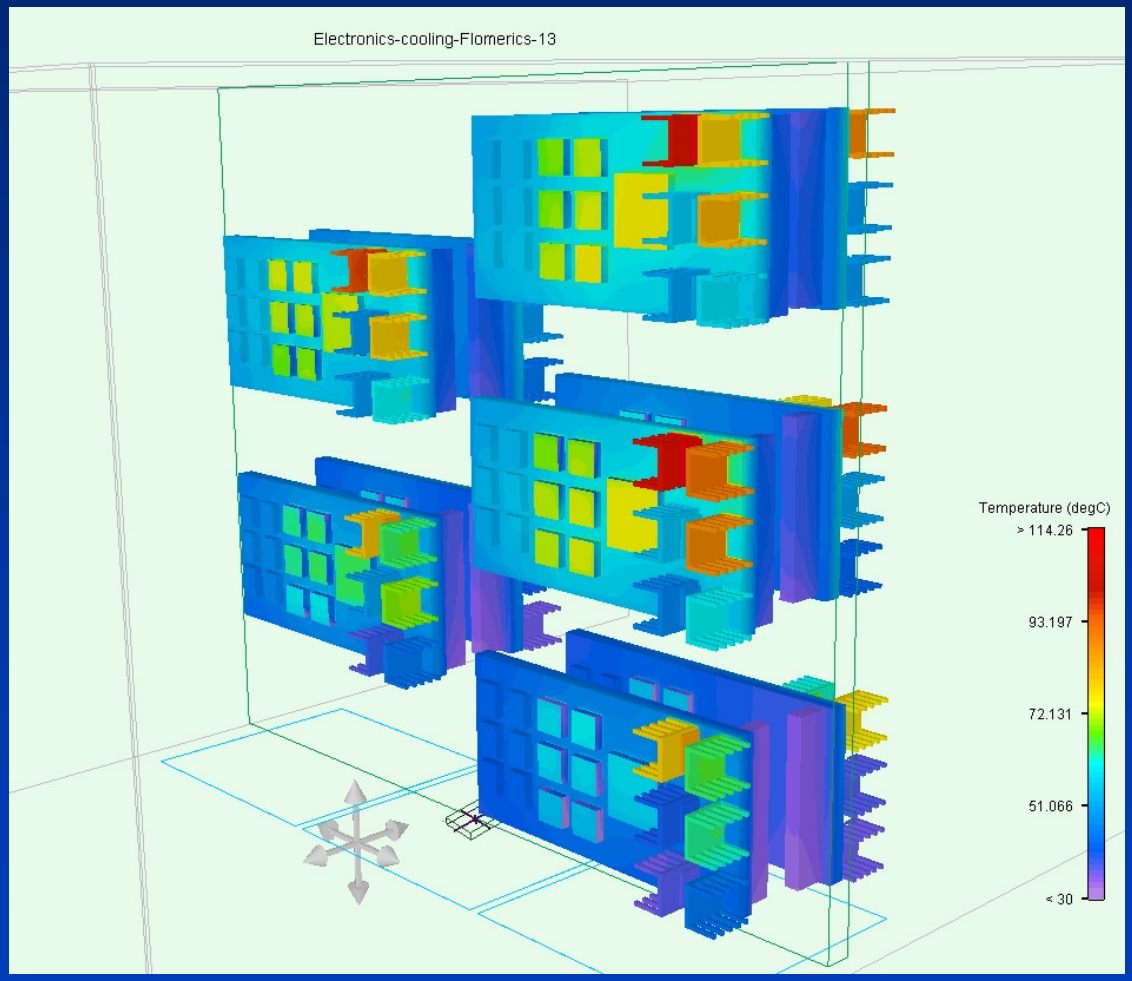
High power density

Thermal verification

FEM simulation with dedicated software

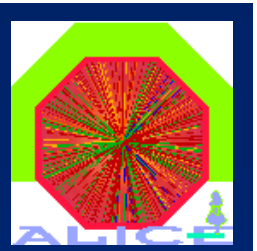
- **Three resistors model for each device**
- **Board and components thermal conductivity**
- **Forced convection**
- **Partially enclosed rack**

Hot spots in acceptable limits



Courtesy: Emile Dupont

Summary



The ALICE Silicon Pixel Detector 1200 Fast-OR signals will be used to generate an input to the CTP for the Level 0 trigger algorithm

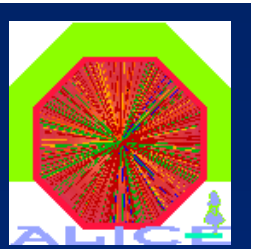
The ALICE experiment will be the first LHC experiment to include from startup its own silicon vertex detector in the Level 0 decision

The Alice Pixel Trigger System is designed and is being constructed

The Pixel Trigger system:

- targets the stringent 800 ns latency constraint
- allows for reconfigurable trigger algorithms
- is independent from the readout chain
- features a modular and upgradeable design:
  - OPTIN optical receiver mezzanine boards with fiber optic receiver modules and G-Link dedicated ASICs
  - BRAIN Processing board based on a large logic and I/O space Virtex 4 FPGA

Spares



Acknowledgements: I.A. Cali', E. P. Dupont, F. Formenti, A. Kluge, M. Krivda, G. Stefanini, F. Vasey, P. Vichoudis,

References:

ALICE collaboration, "*ALICE physics Performance Report*", CERN-LHCC-2003-049, J. Phys., G30 (2004) 1517-1763

A. Kluge, "*The ALICE Silicon Pixel Detector front-end and readout electronics*", NIM A 560 (2006) 67-70

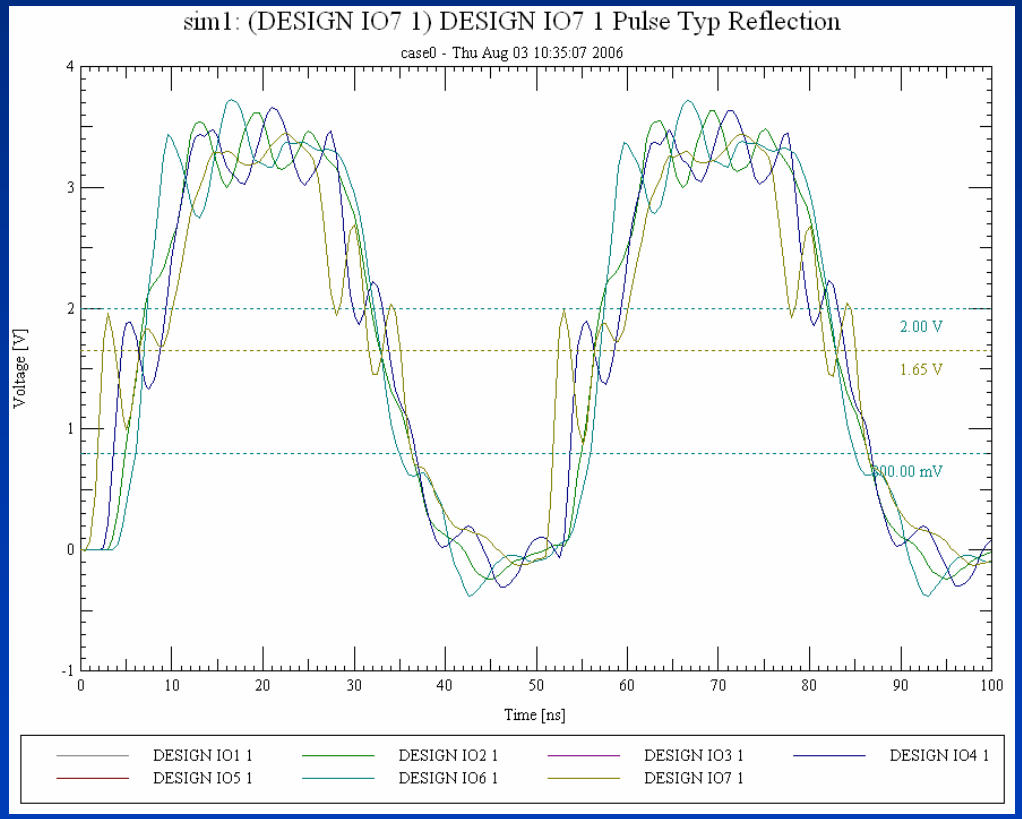
M. Krivda*, "Alice SPD readout electronics",* proceedings of this conference

J. Conrad et al., "*Minimum Bias Triggers in Proton-Proton collisions with the VZERO and Silicon Pixel Detectors*", ALICE Internal note, ALICE-INT-2005-025, 19/10/2005

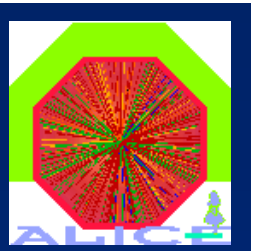
Signal integrity studies

Signal integrity studies on the communication buses

- IBIS models of the Virtex 4 output buffers
- Physical parameters of the board striplines



Radiation effects



Neutron max fluence: 2.0 • 10^8 cm^{-2} (10 y)

Morsch, Pastircak, *Radiation in ALICE Detectors and Electronic Racks*, ALICE-INT-2002-28

Central Trigger Processor using SRAM based ALTERA Cyclone EP1C20

***Radiation Results of the SER Test of Actel, Xilinx and Altera FPGA instances,* iROC report, 2004**

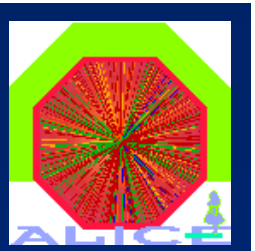
Failure In Time (FIT): errors in 10^9 years
SEFI: Single Event Functional Interrupt
SEU: Single Event Upset (configuration)

FIT	SEFI	SEU
Altera EP1C20	453	
Xilinx XC3S1000	320	1240
Xilinx XC2V3000	1150	8680

Errors in 10 years operation

Errors	SEFI	SEU
Altera EP1C20	6	
Xilinx XC3S1000	5	18
Xilinx XC2V3000	16	124

Trigger latencies and rates



	Level 0	Level 1	Level 2
Last trigger input at CTP (μs)	0.8	6.1	87.6
Trigger output at CTP (μs)	0.9	6.2	87.7
Trigger input at detectors (μs)	1.2	6.5	
Rate (Hz)		1000	40-800

Time resolution

SPD time resolution: 100 ns
Pileup of event data in p-p interactions at 25 ns bunch crossing rate