The Level 0 Pixel Trigger System for the ALICE experiment: implementation, testing and commissioning

Gianluca Aglieri Rinella[1]

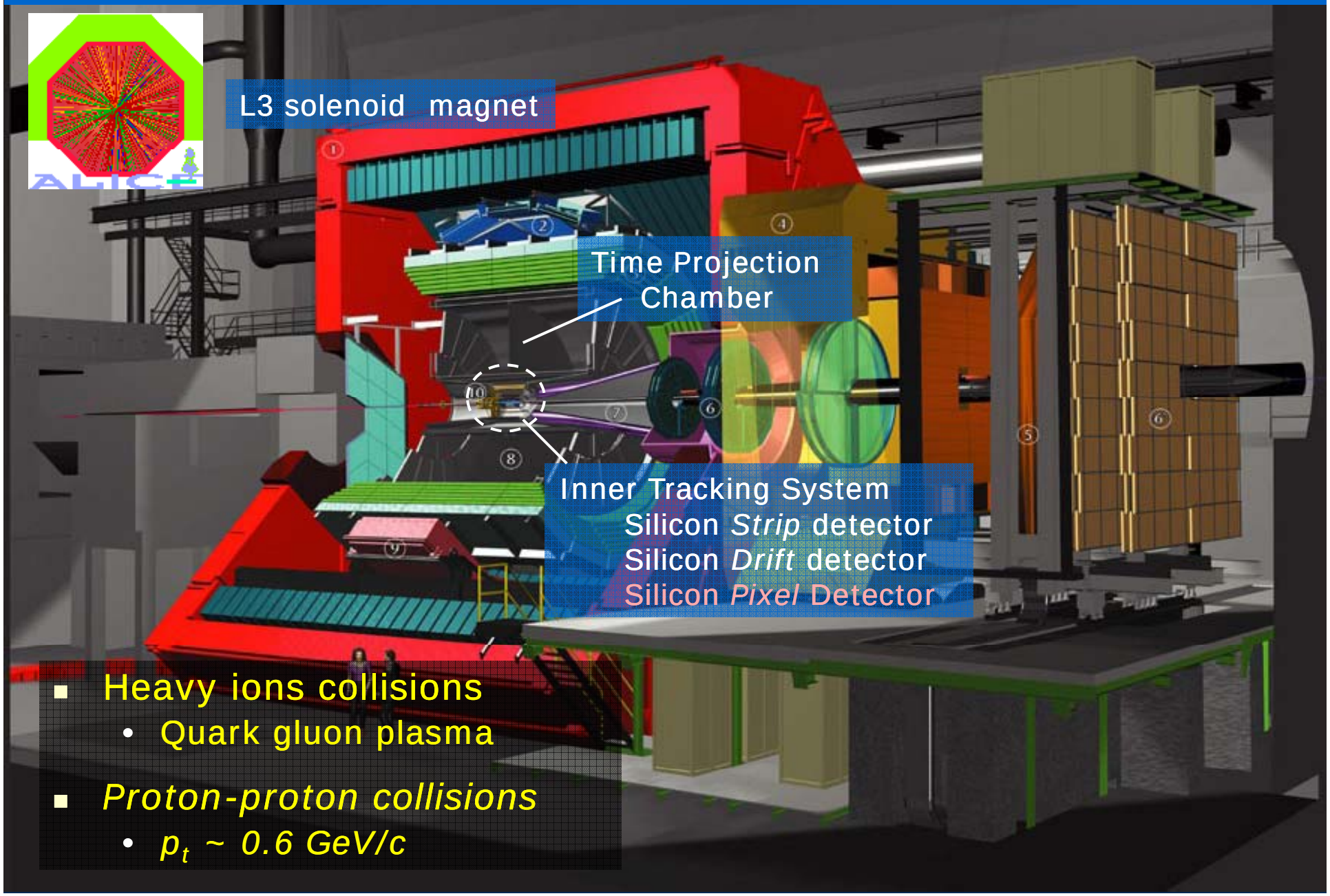
On behalf of the ALICE Silicon Pixel Detector Team

[1]*CERN, European Organization for Nuclear Research*

Outline

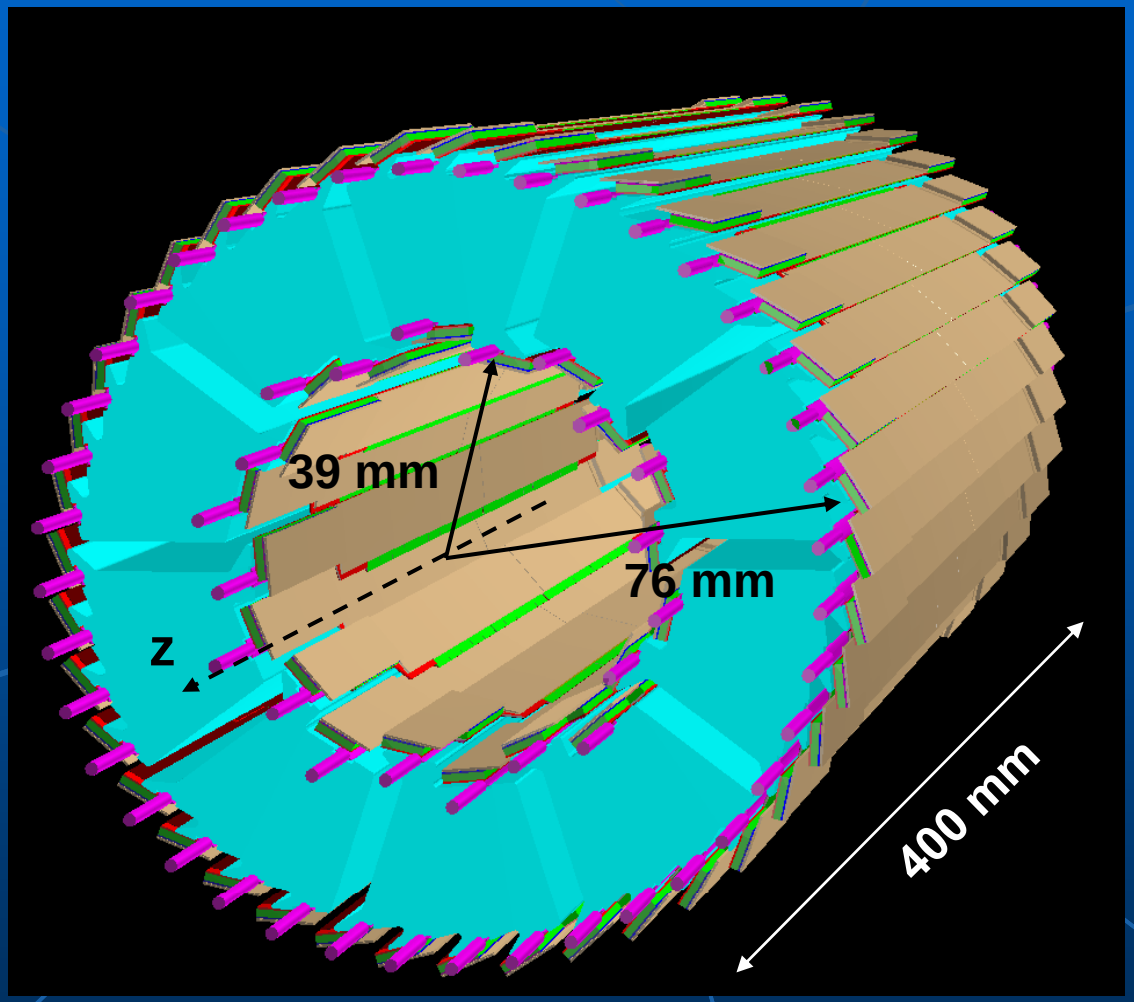
- ALICE Silicon Pixel Detector
  - Detector modules
  - Fast-OR signals
- Pixel Trigger System
  - Description
  - Features
  - Tests and qualification
  - Commissioning
- First operation

The ALICE experiment at LHC



- Heavy ions collisions
  - Quark gluon plasma
- *Proton-proton collisions*
  - p_t ~ *0.6 GeV/c*

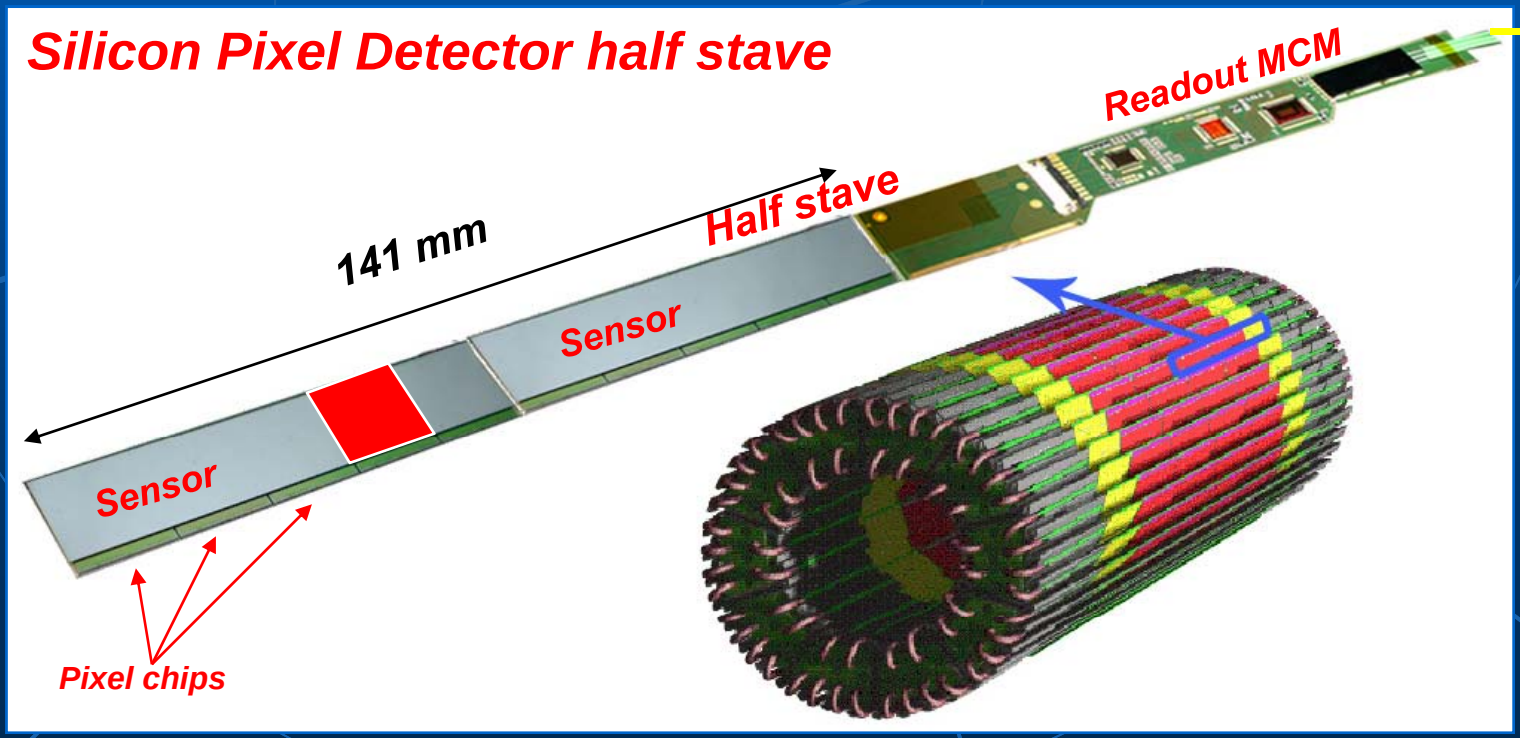
Silicon Pixel Detector



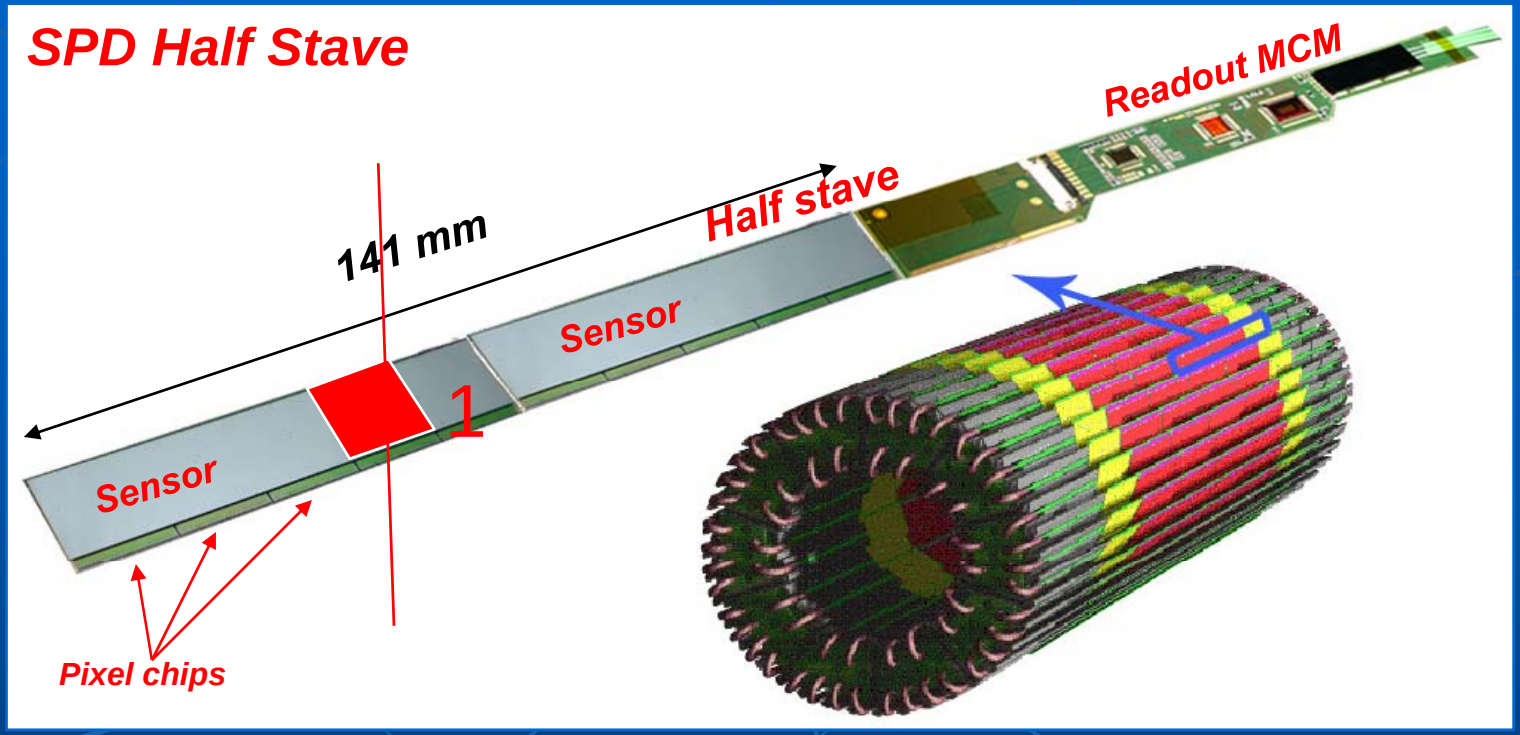
- 120 detector modules (*half staves*)

SPD half stave

- Each half stave (120):
  - Si pixel sensors (pixel size 425x50 $um^{2)}$
  - 10 readout pixel chips (32x256=8192 pixels)
    - *10 MHz*
  - Readout Multi Chip Module
    - *40 MHz*
    - Provides 10 MHz to pixel chips



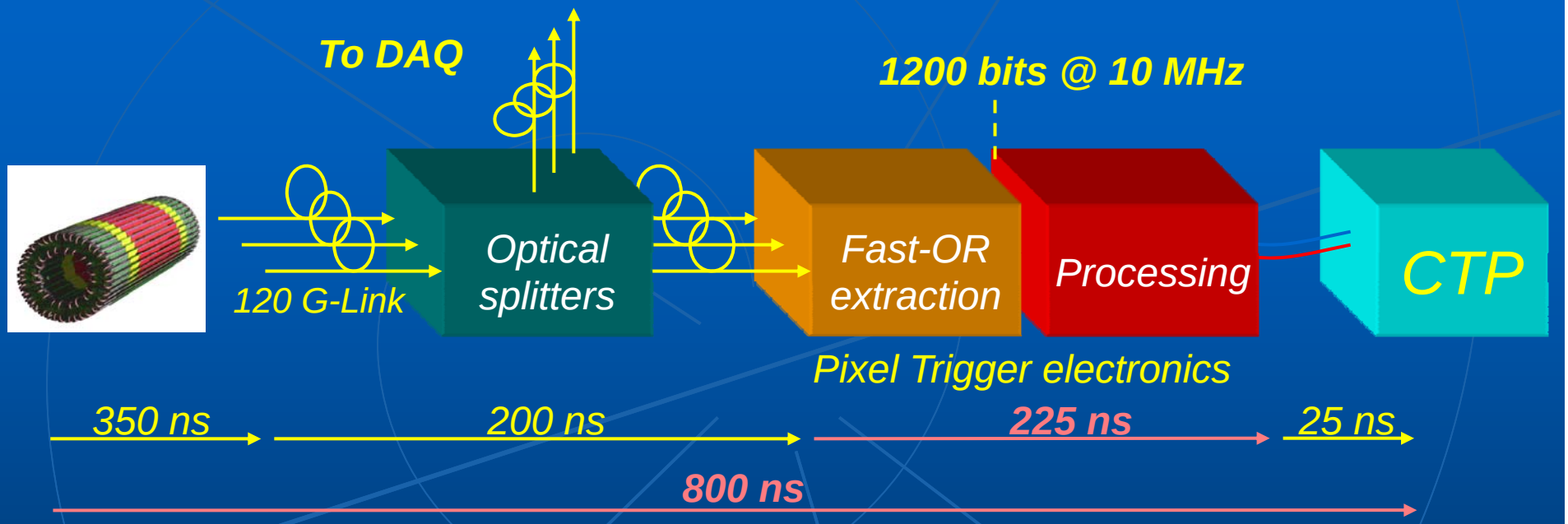
Fast-OR signals



- Pixel chip prompt Fast-OR
  - Active if at least one pixel hit in the chip matrix
  - 10 on each of 120 optical links (1200)
  - Transmitted every 100 ns
- Low latency pad detector

  1200 pads of 13x14 mm^2

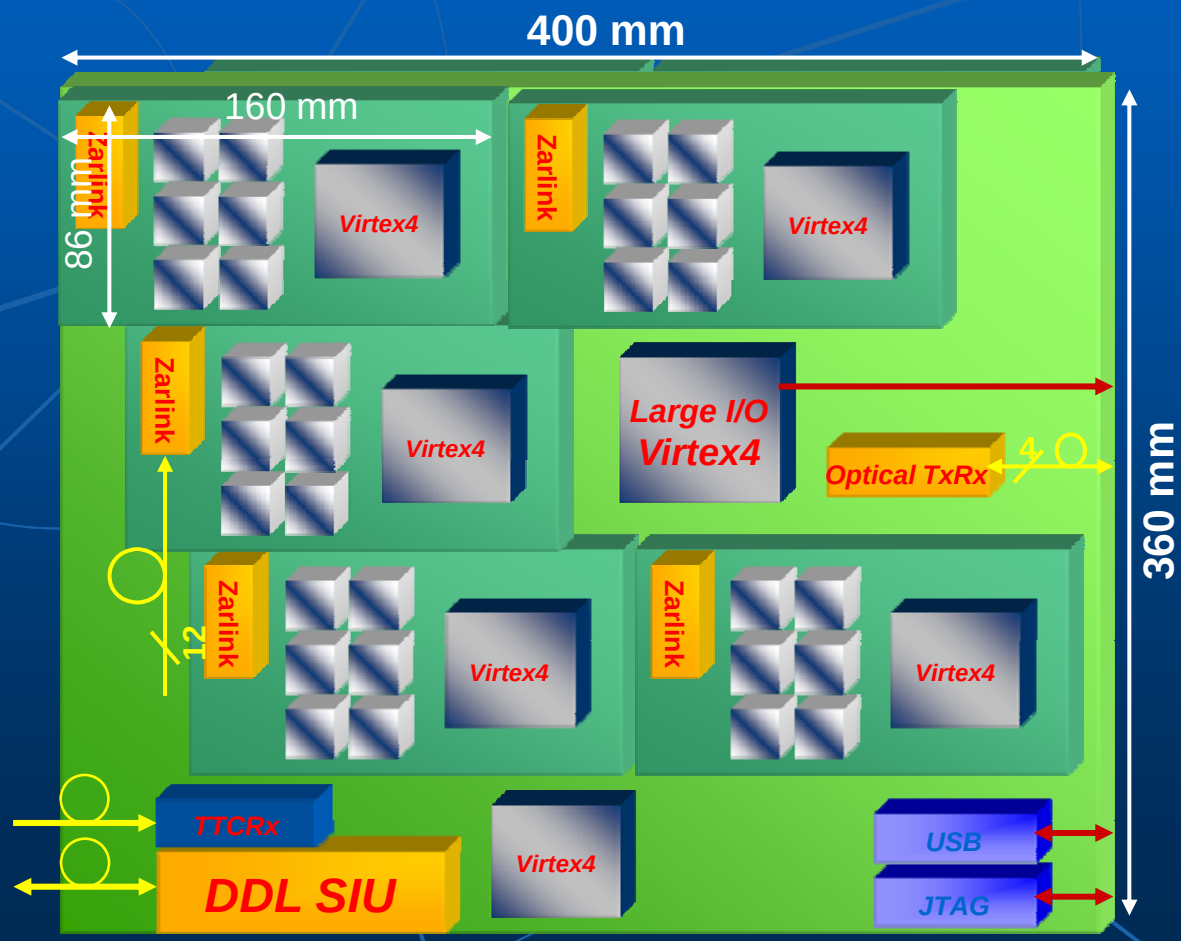
Pixel Trigger System



- Overall latency: **800 ns**
- Space occupancy (1 crate)
- Bottleneck: data deserialization and Fast-OR extraction
  - Processing time < 25 ns

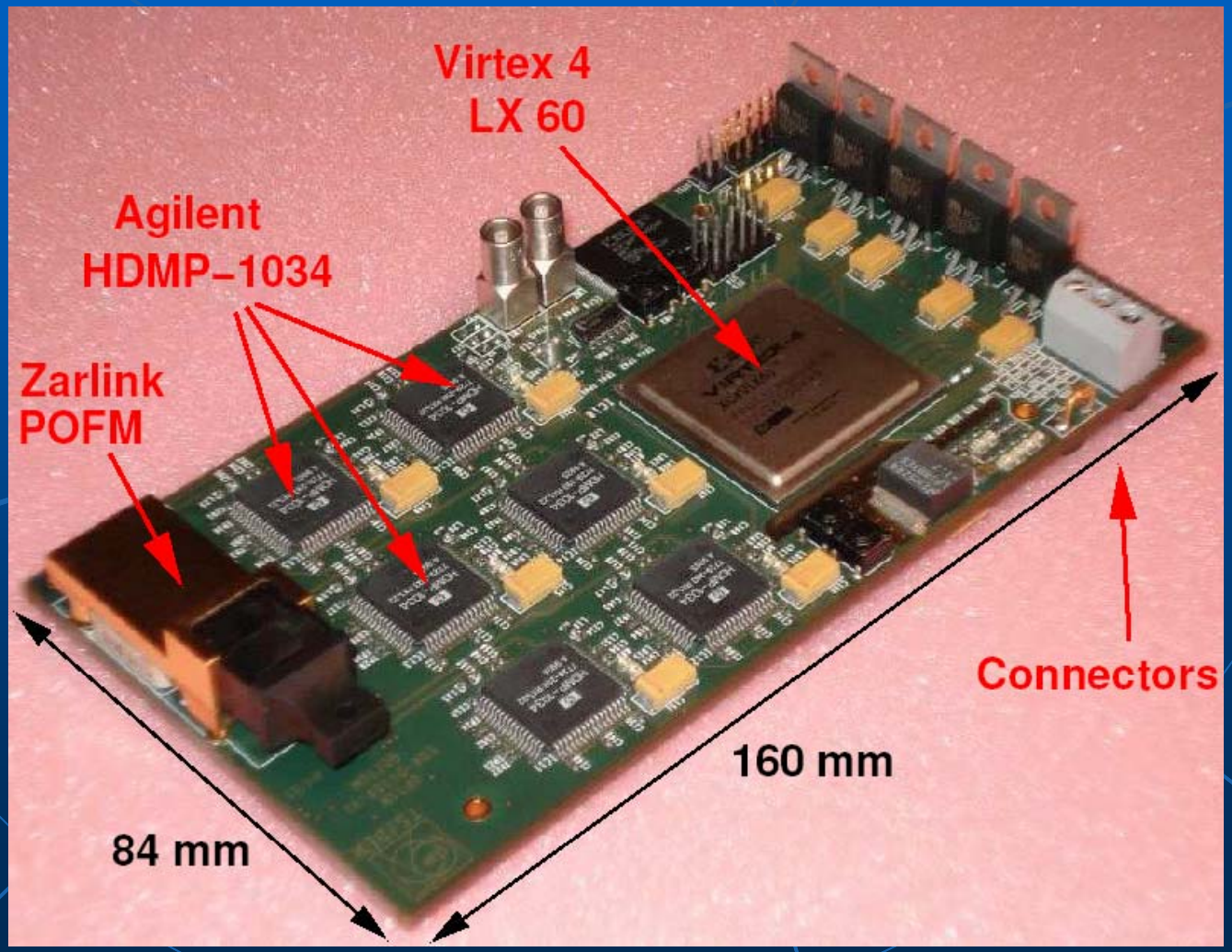
Pixel Trigger system electronics

- 9U VME size processing board (BRAIN)
  - Main processing FPGA (960 user I/O pins, 1513 BGA)
- 2x5 receiver boards (OPTIN) connected as mezzanine boards
- High speed optical interfaces
  - Alice Detector Data Link
  - Timing Trigger
- Data flow parallelism (~1000 lines)
  - 800 impedance matched lines
  - Digitally Controlled Impedance
  - Double Data Rate

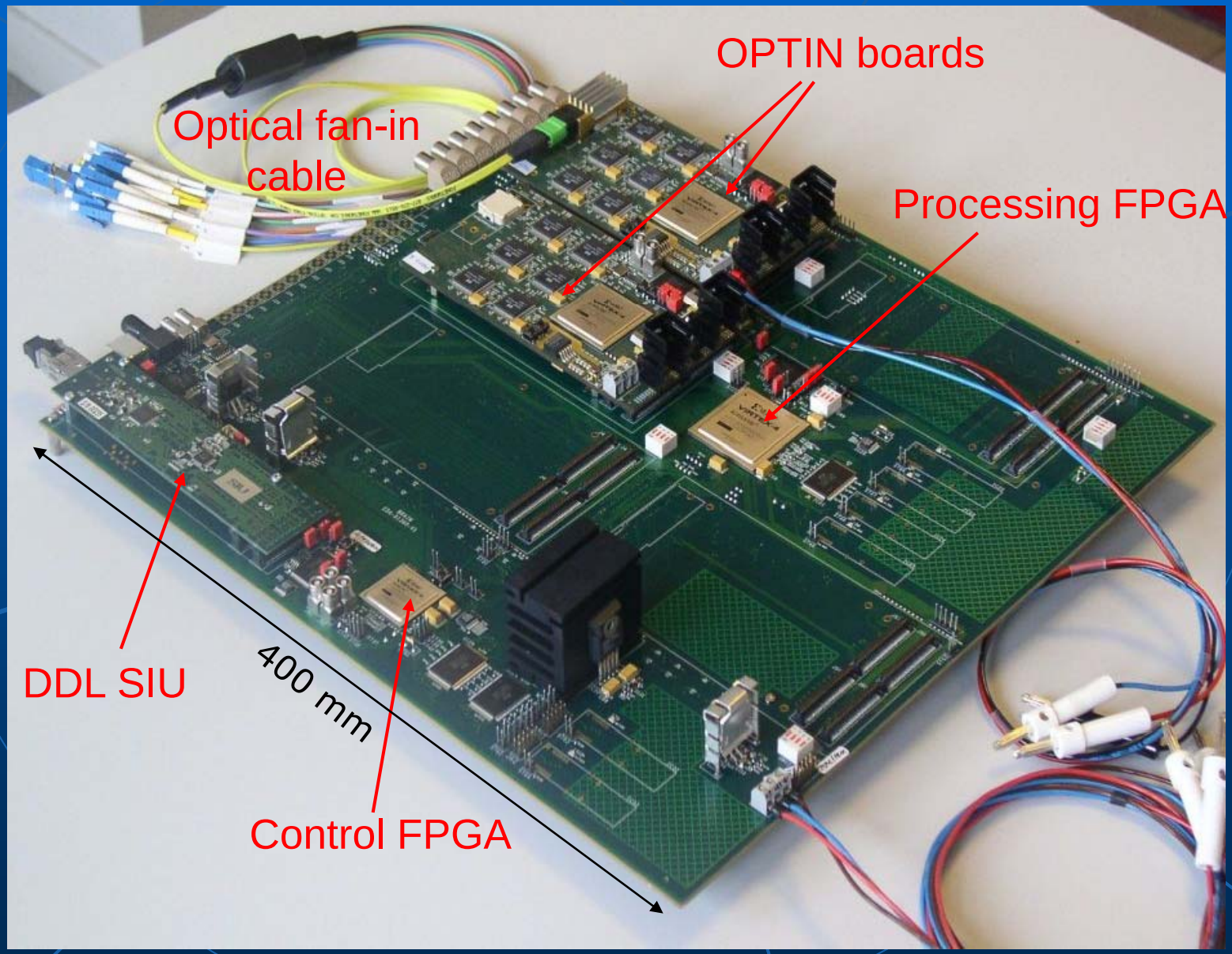


OPTIN receiver board

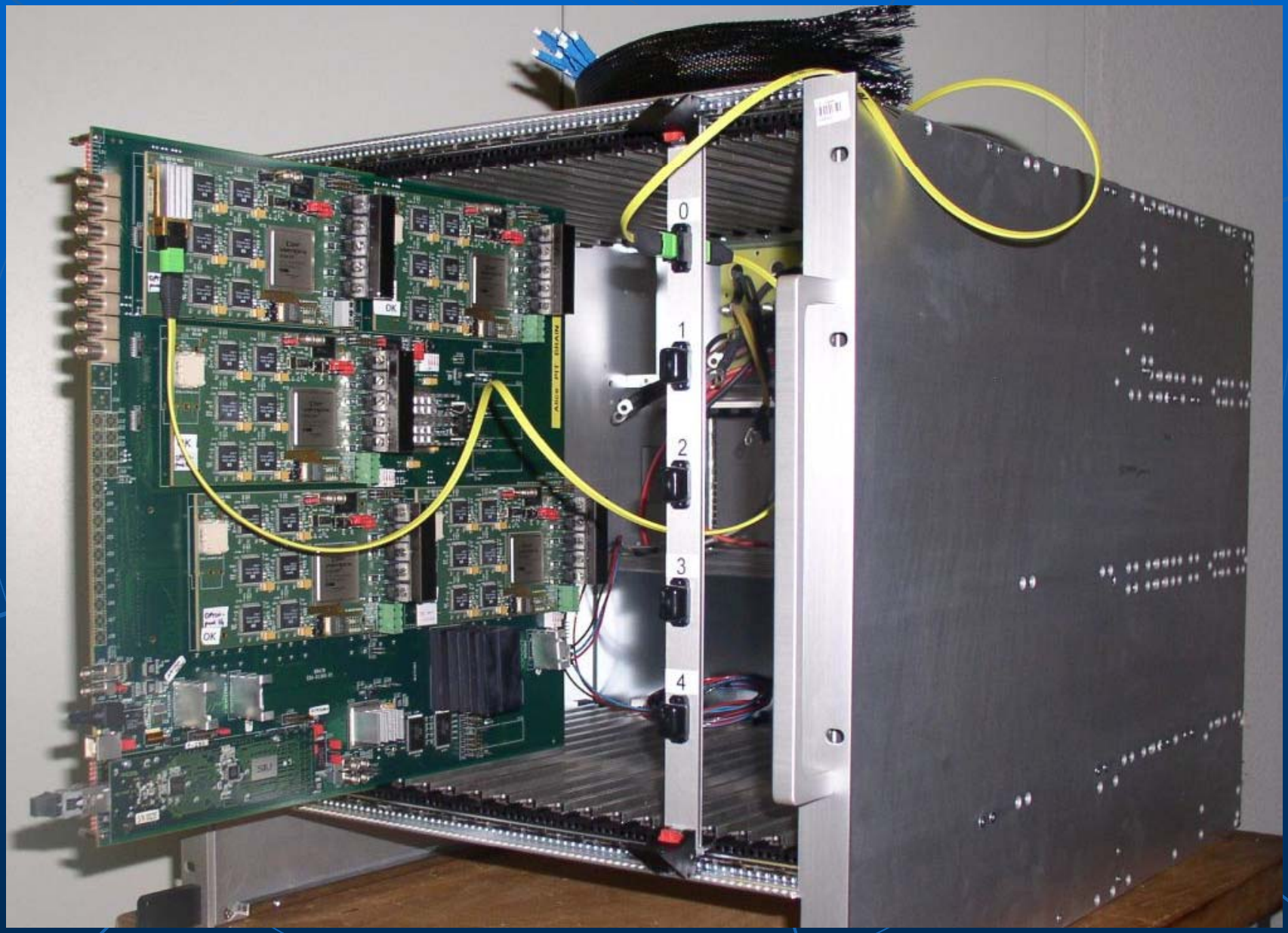
- 12 channels
  - Parallel optical receiver module
  - 12 closely packed G-link deserializer ASICs



BRAIN and OPTIN boards



Pixel Trigger system crate



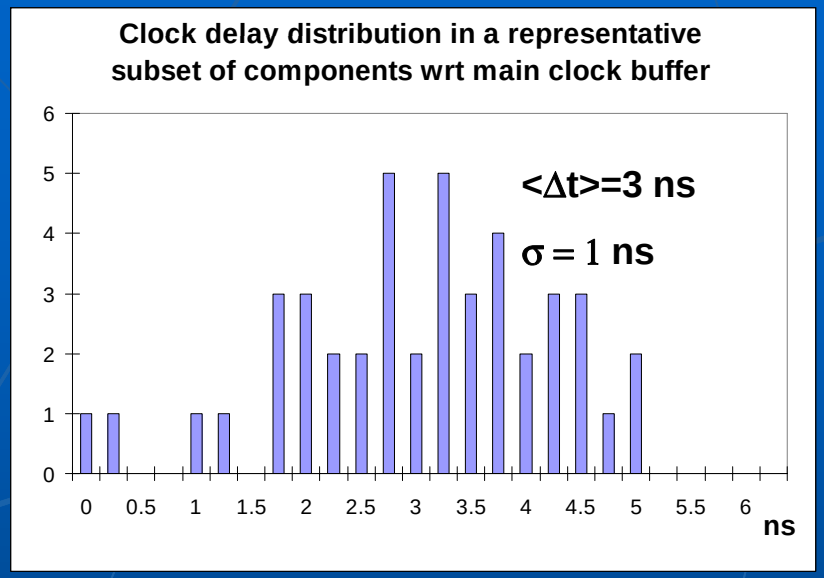
Interconnection test and power consumption

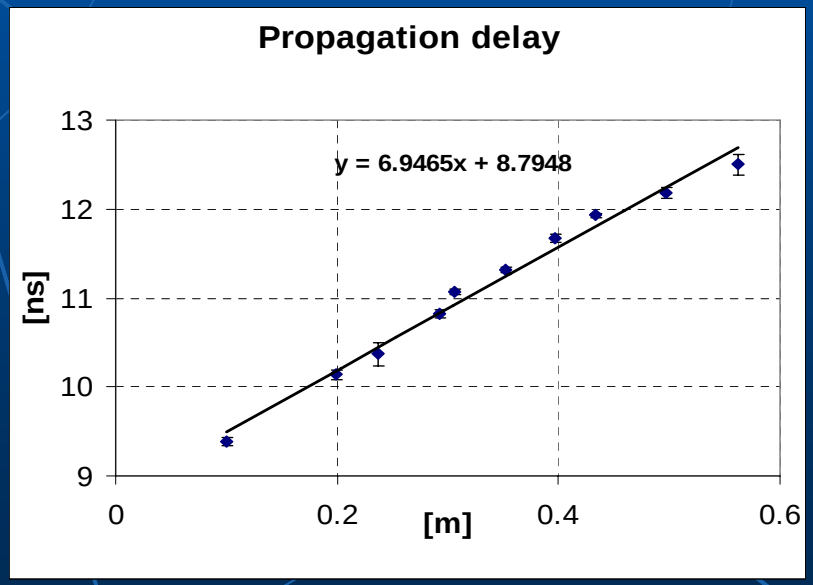
- Electrical interconnects
  - Full JTAG testing
  - Dedicated tests for
    - lines non accessible by JTAG
    - high speed differential lines
- Heat sinks on all regulators and deserializers
  - Peak board temperature: 45 °C (measured)
  - Peak junction temperature: 72 °C (thermal model)
- Currents overestimated in design phase
  - Thermal model was *too conservative*

	I_{5V} [A]	$I_{3.3V}$ [A]	**P [W]**
OPTIN	2.8	0.375	**15.3**
BRAIN	7.9	1.6	**45**
Total PIT	36.1	5.4	**198**

Clock distribution

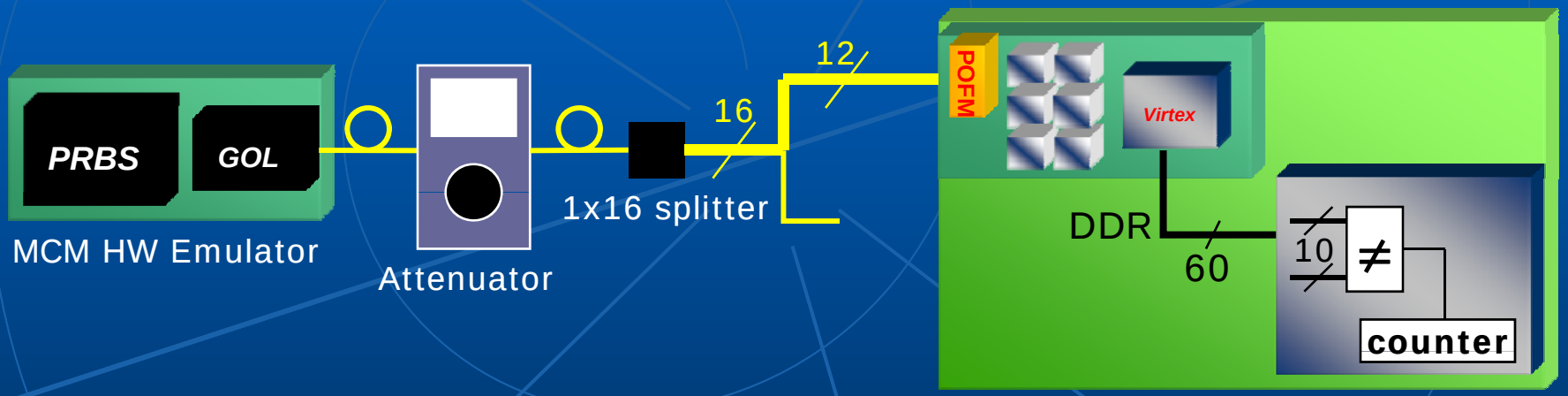
- Measurement of phase distribution
- Processing FPGA clock
  - Phase correction in order to place it at the centre of the distribution
  - Digital Clock Management
- Measured signal propagation delay
  - Design: 7.8 ns/m
  - Measured: 6.95 ns/m





Optical link BER tests

- Full Fast OR data path Bit Error Rate test
  - 12 channels in parallel, each OPTIN tested sequentially
  - Pseudo random data
  - Link optical power: **-18.5 dBm**, 0.5 dBm margin

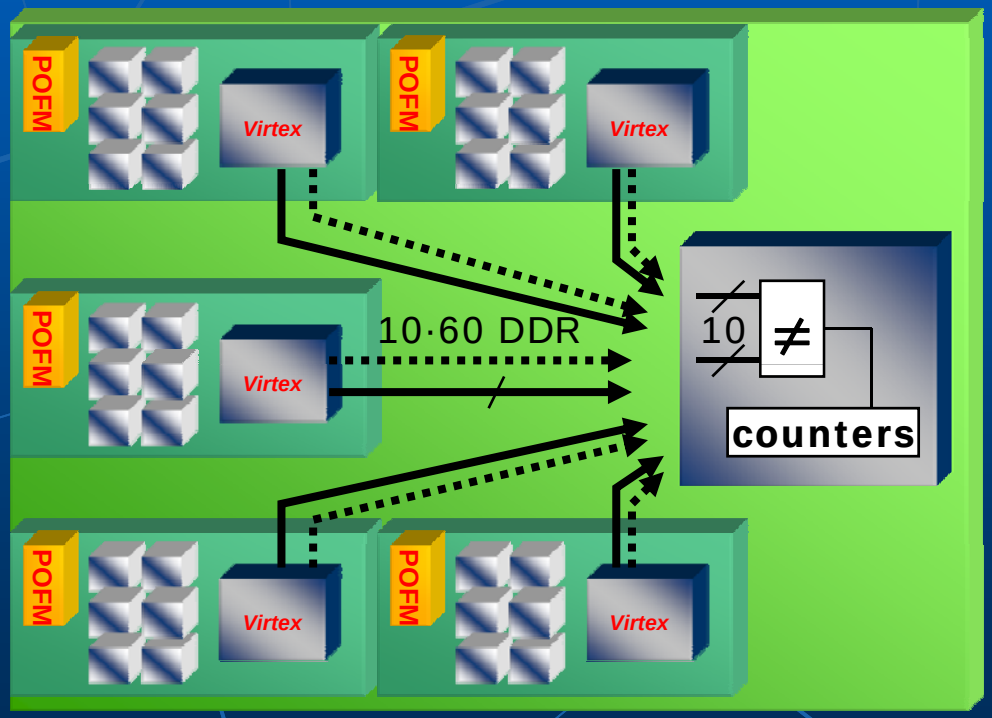


	Duration	N_{bits}	Errors	BER (99% c. l.)
Typical	1.5 hrs	$5.7 \cdot 10^{12}$	0	**$< 8.1 \cdot 10^{-13}$**
Max	17.8 hrs	$7.7 \cdot 10^{13}$	0	**$< 6 \cdot 10^{-14}$**

Fast OR data path integrity

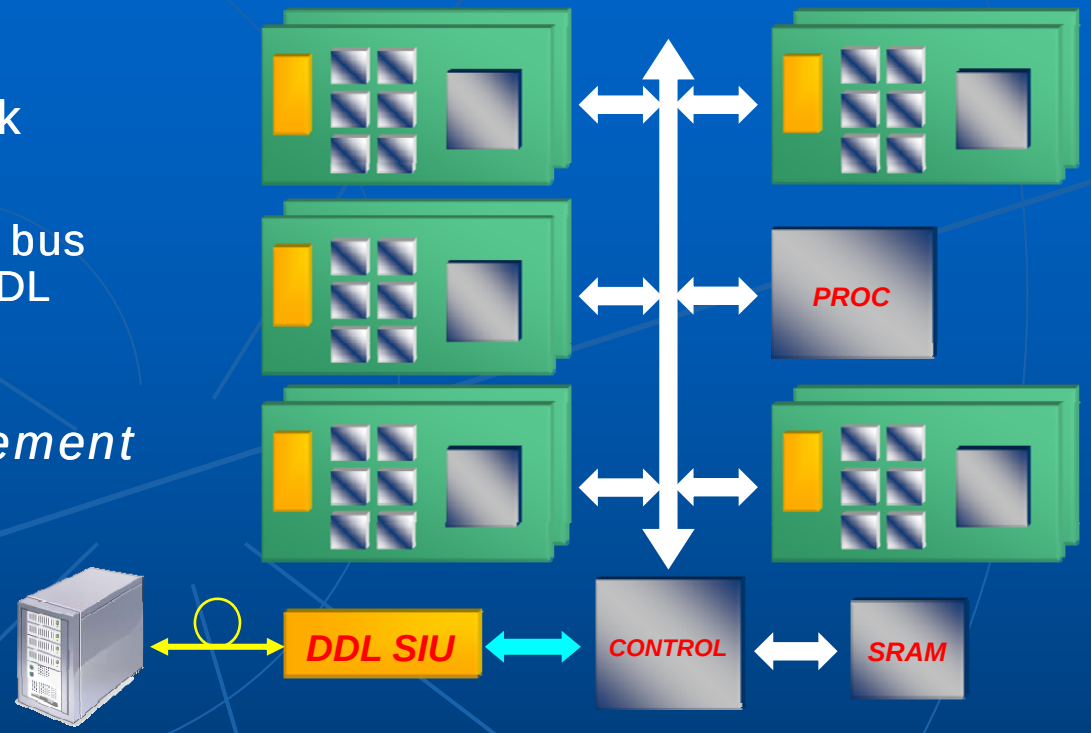
- Fast OR dedicated lines (600) Bit Error Rate test
  - 10 OPTIN boards, 120 channels simultaneously running
  - On board generation of User Defined data functionality (pseudo random sequences)

- Duration: 15 hrs
  - $N_{bits} = 6.48 \cdot 10^{14}$
  - Errors = 0
- BER < $\mathbf{7.1 \cdot 10^{-15}}$ (99% c.l.)



Pixel Trigger system control

- Custom control interface
  - ALICE Detector Data Link
  - On board PCI like bus
    - CONTROL FPGA acts as bus master and bridge to DDL
- Reliability
  - Transaction *acknowledgement*
  - *Parity* checking
  - *Error recovery*

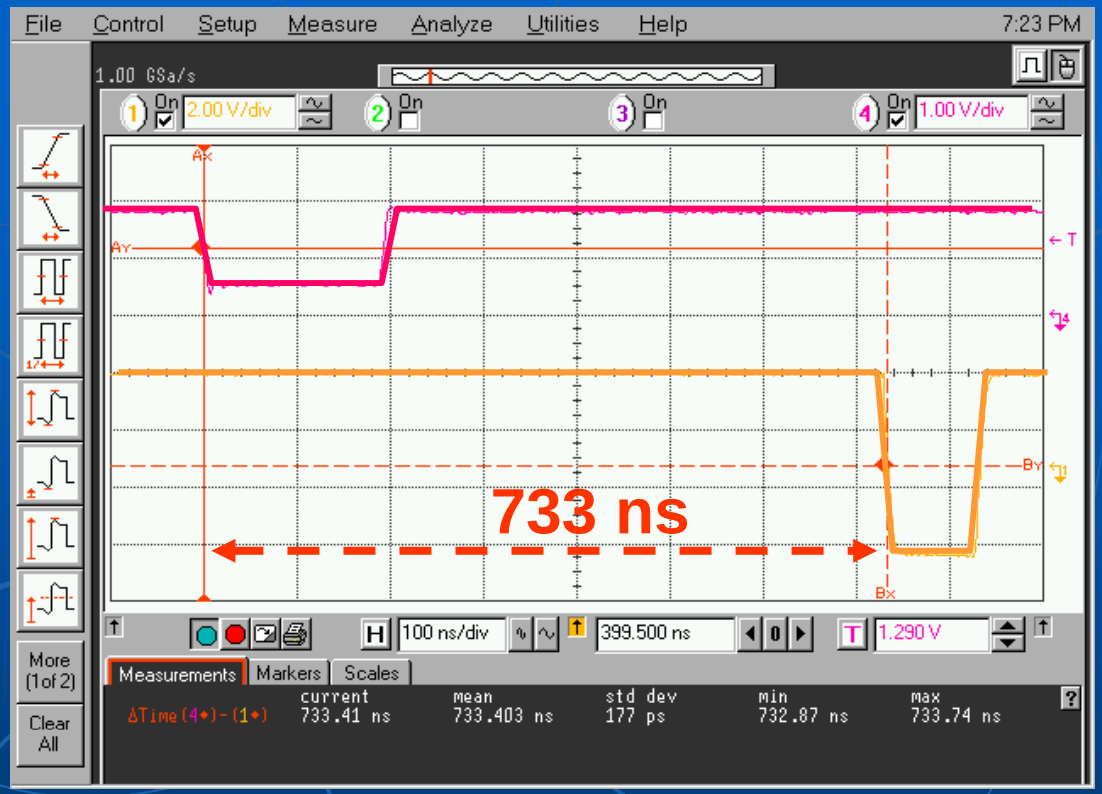


- Read/write test pseudo-random data
  - Typical duration: 15 mins, ~$6 \cdot 10^8$ bits exchanged, 0 errors
  - Longest: 12 hrs, ~ $3 \cdot 10^{10}$ bits, 0 errors
- See poster by Cesar Torcato Matos

Latency measurement

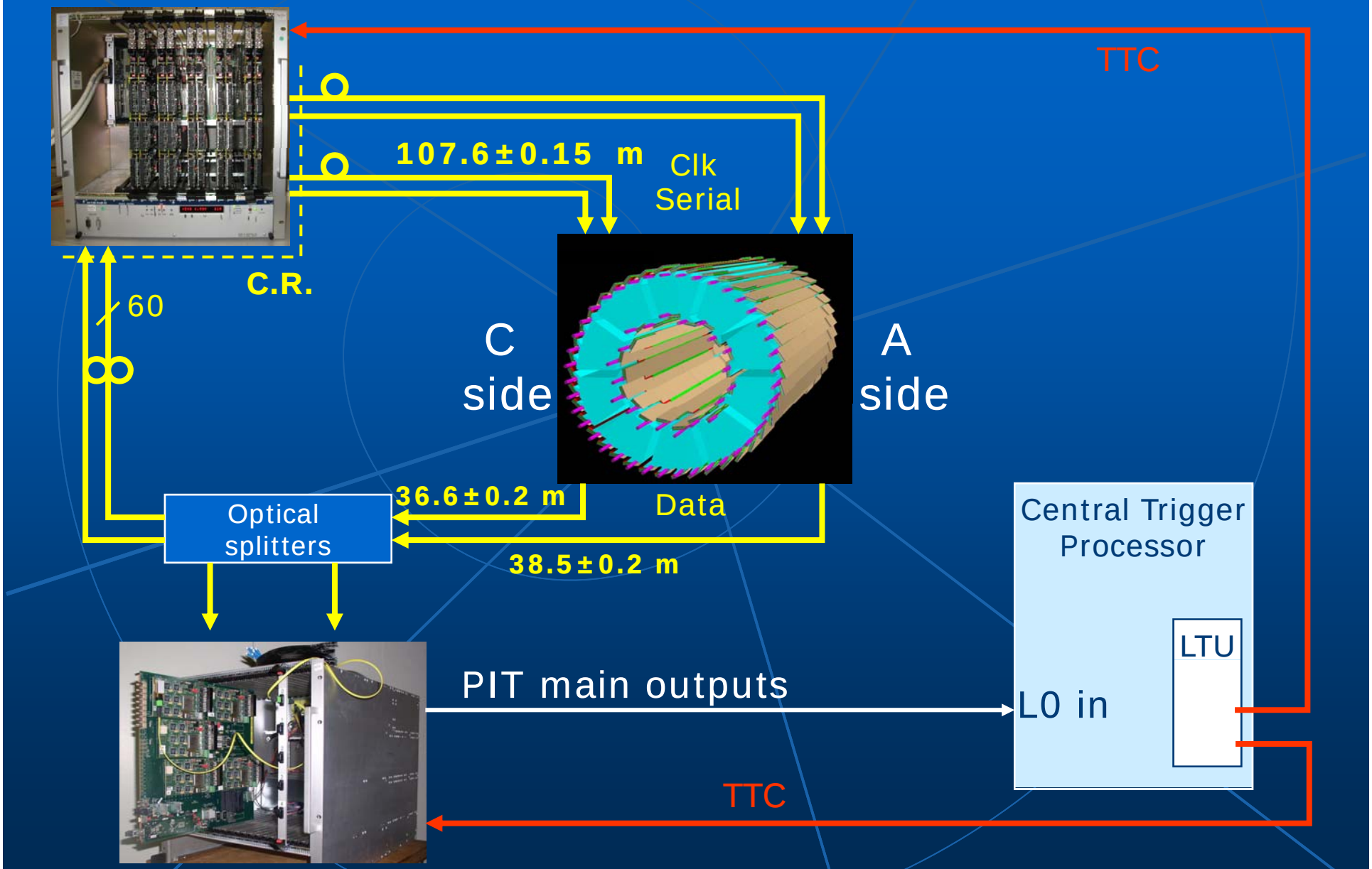
Test pulse ->

PIT output ->

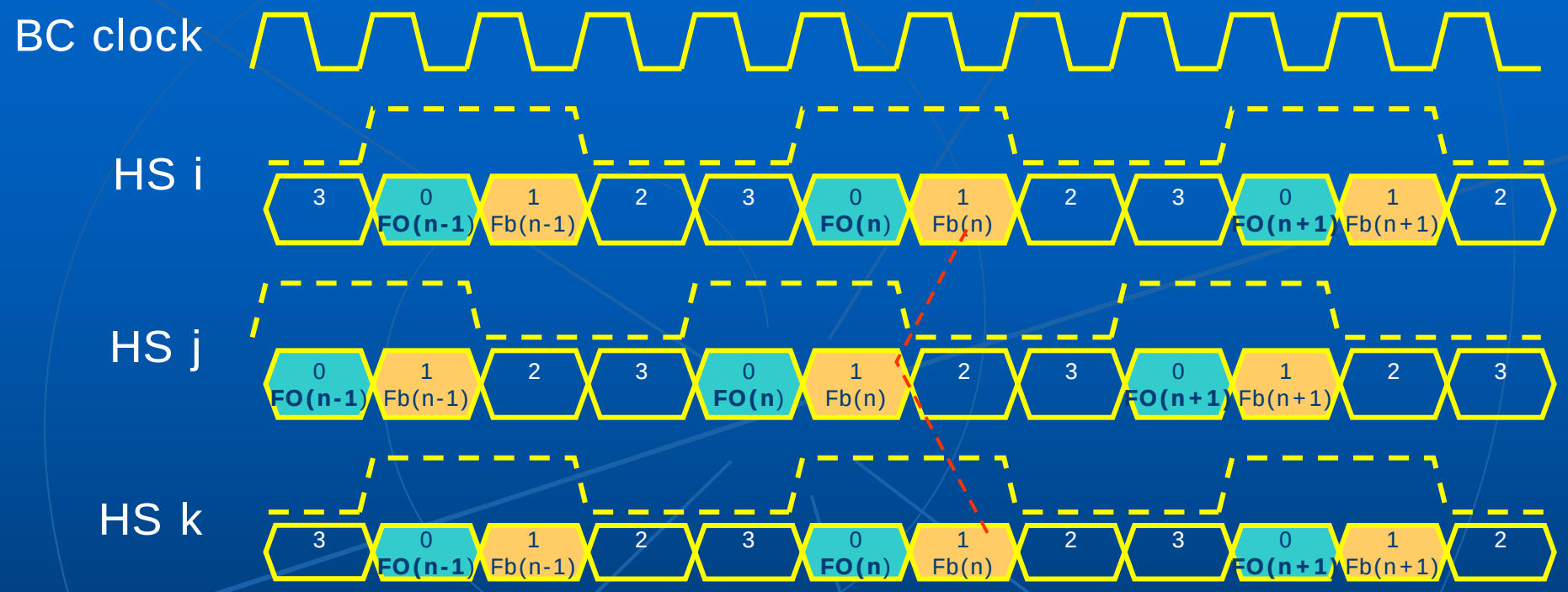


- Laboratory measurement
- In ALICE
  - *768 ns* (best case)
  - *<u>793 ns</u> (realignment)*

Installation in ALICE experiment



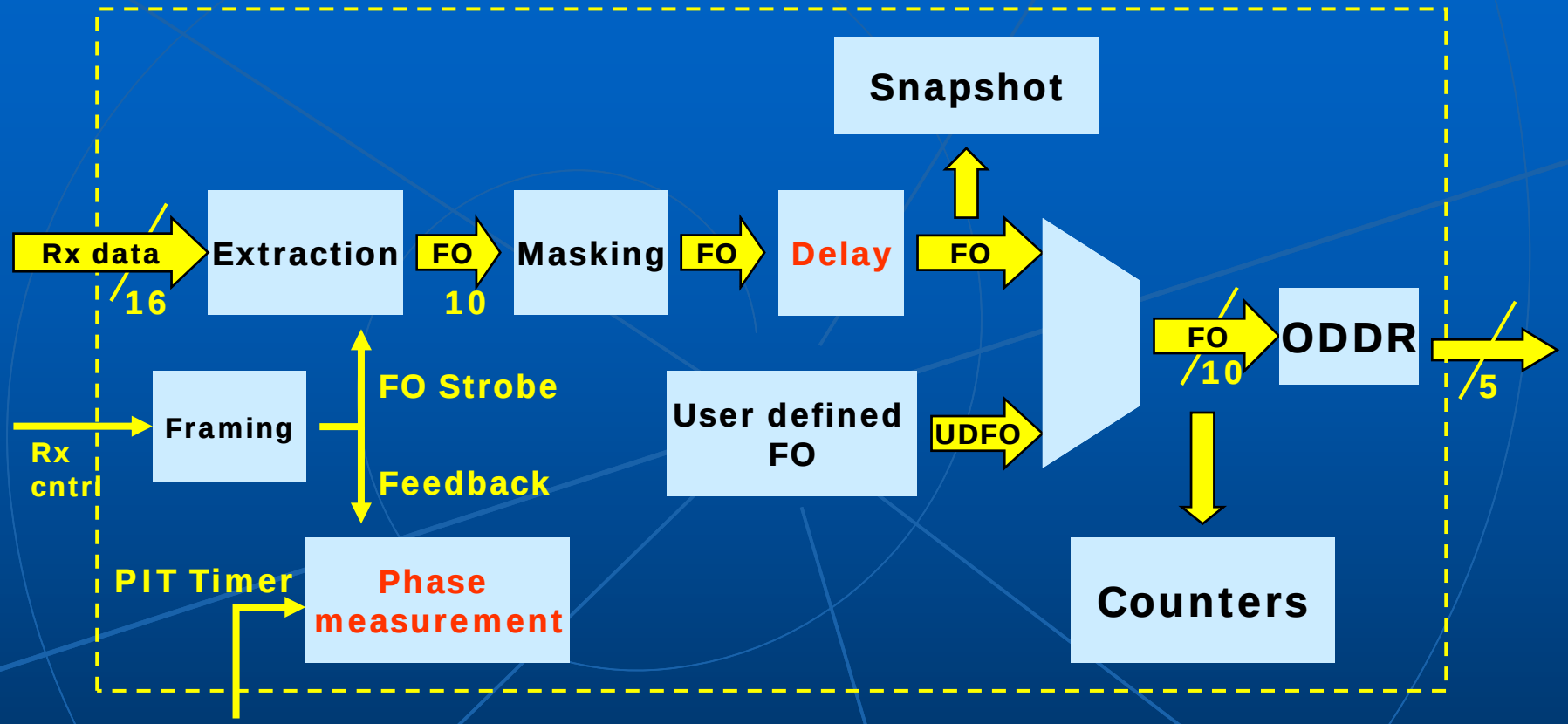
Synchronization



- 40 MHz clocks aligned by equalizing fibers length
- 10 MHz clock phases aligned by broadcast signal on TTC

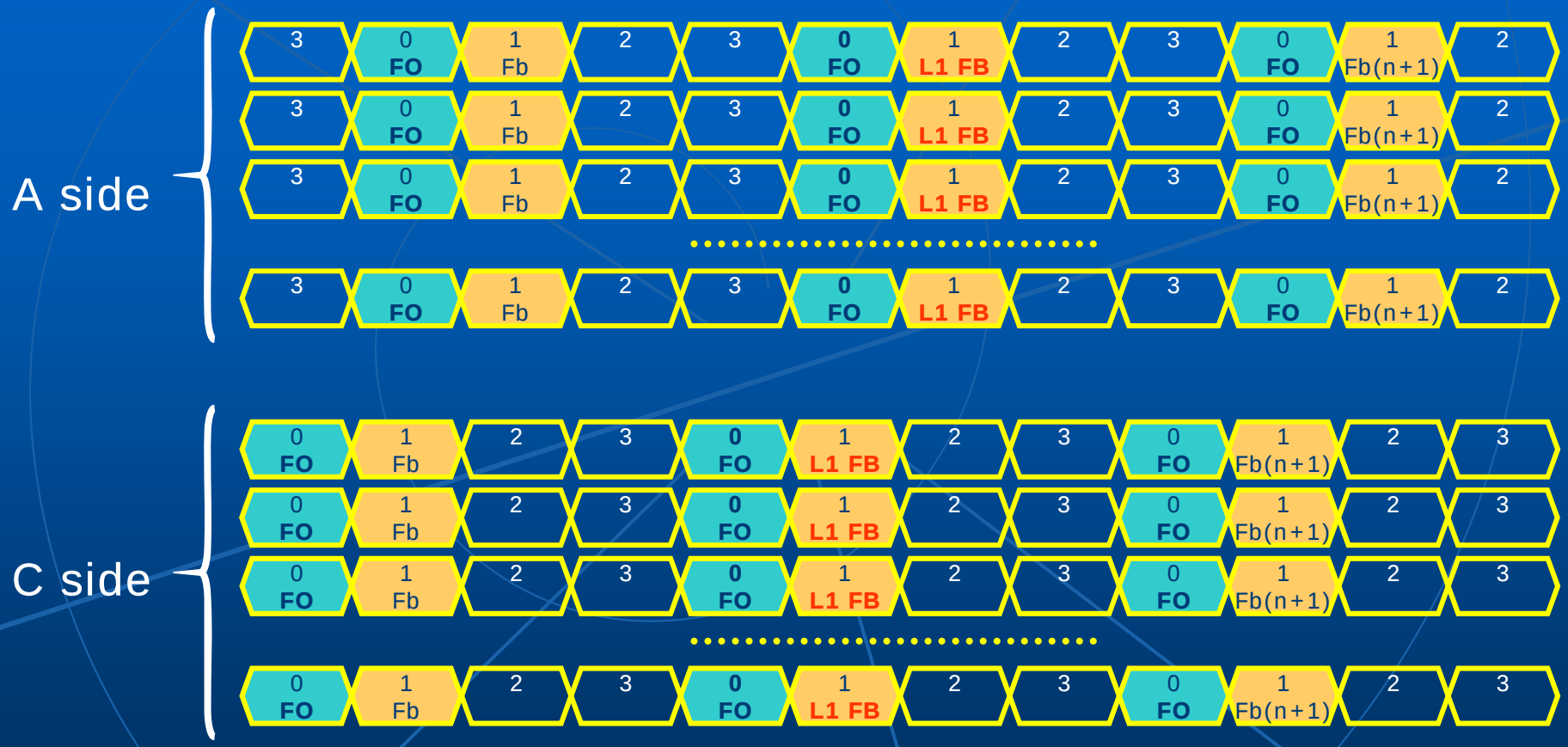
- One clock period uncertainty left -> Measure relative phases
  - ***Measure arrival time of trigger feedback***

OPTIN receiver board channel



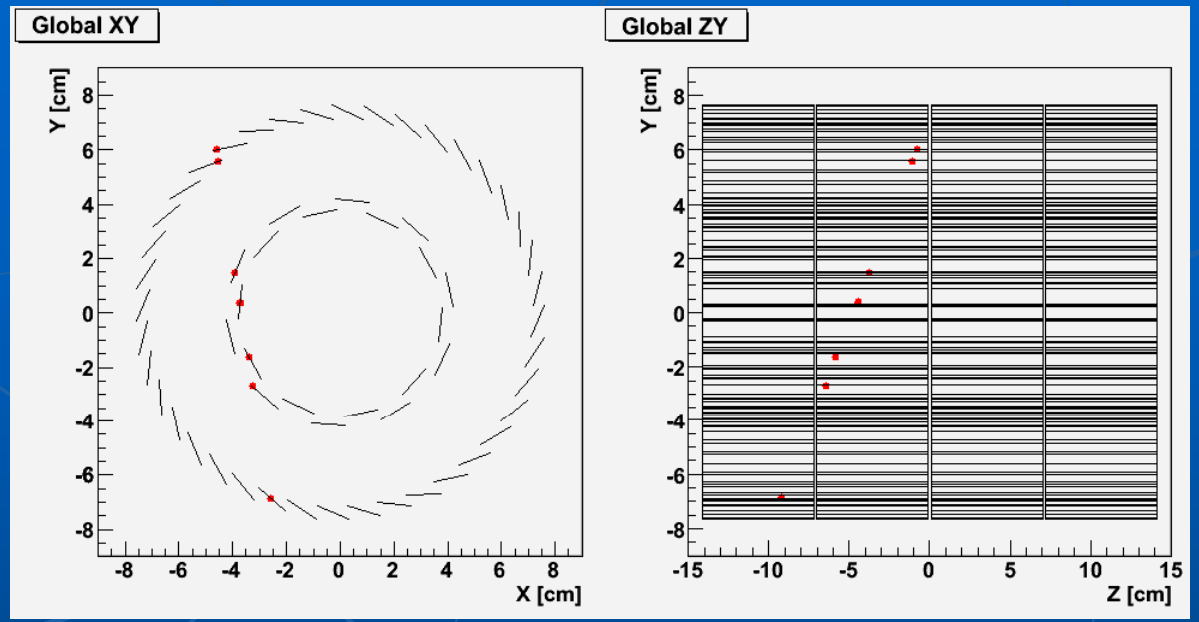
- Trigger feedback arrival clock period is time stamped
- Discrete delay can be added to compensate for misalignments
- Automatic driver function to measure latencies and set delay

Frame alignment

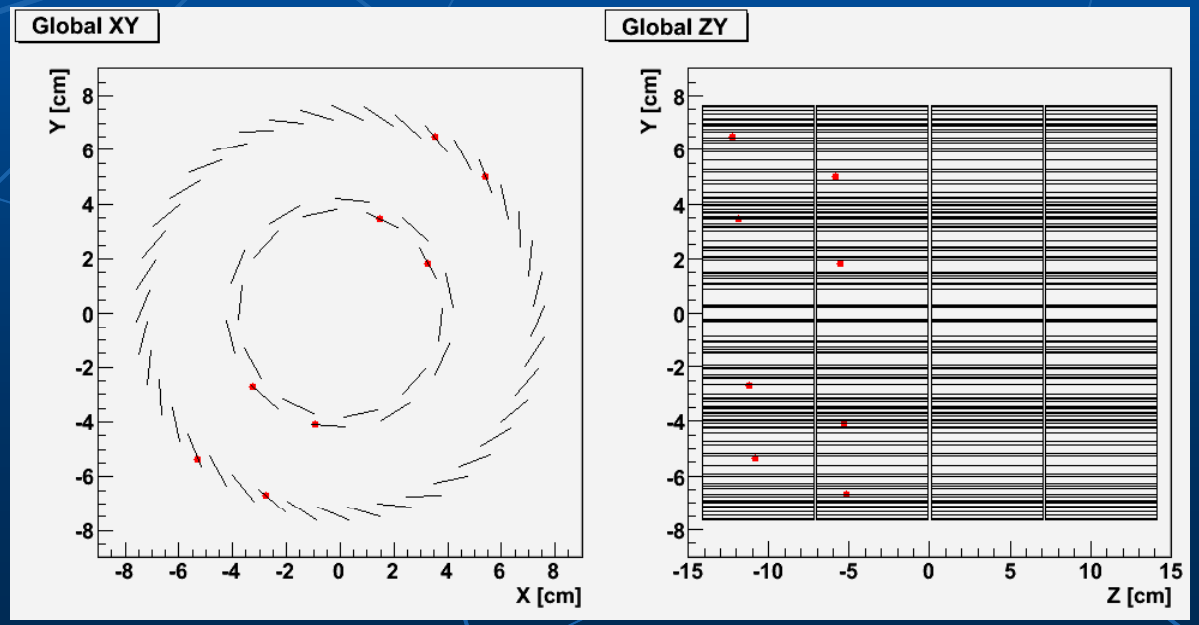


Cosmic radiation in the cavern

- Pixel trigger used for cosmic data taking
  - SPD only
  - ALICE (ITS + TPC)

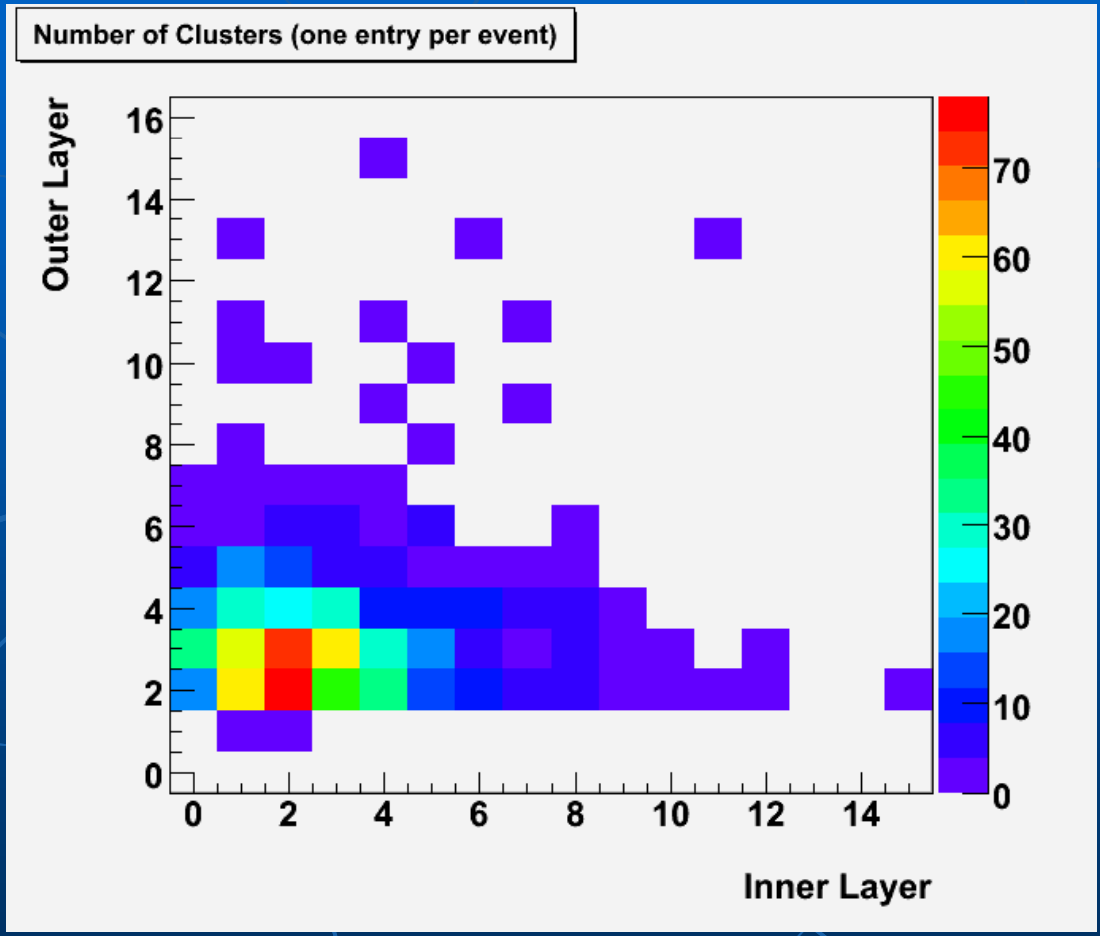


- Alignment data
  - 65000 events ≥ 3 clusters in SPD
  - 35000 events ≥ 4 clusters in SPD
  - Showers



Cosmic data clusters

- Rate 0.09 Hz – 0.12 Hz
  - Well in agreement with Monte Carlo and measured flux in the cavern
- Cluster distribution
  - 99.5 % of events with correct cluster distribution



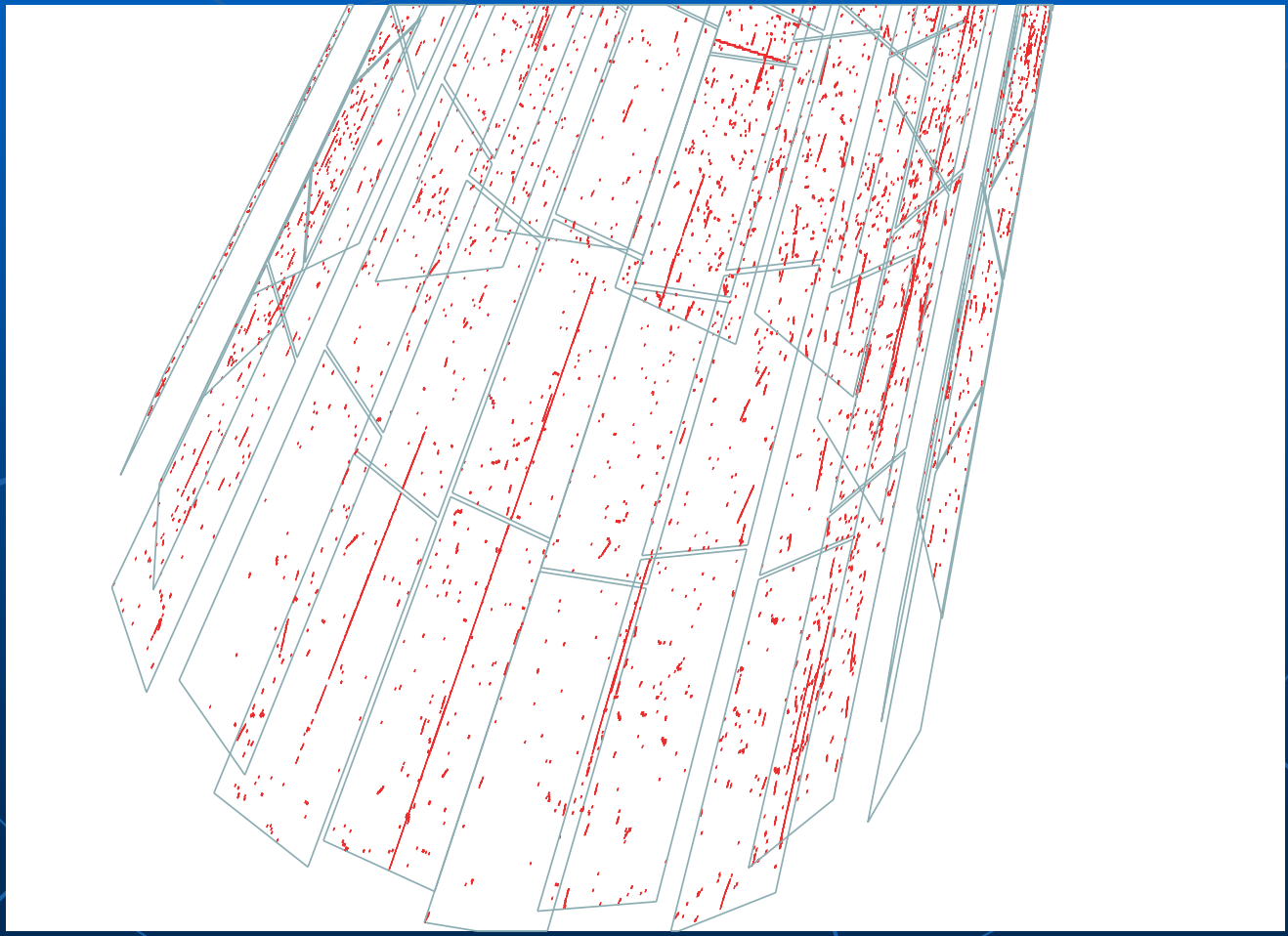
Summary

- The ALICE Pixel Trigger system allows to include the prompt Fast-OR outputs of the Silicon Pixel Detector in the Level 0 trigger decision
  - ALICE is the only LHC experiment including the vertex detector in the first trigger decision from startup
- The Pixel Trigger system
  - Installed and operational
  - Board level and system level challenging requirements
  - Highly compact solution including original developments
  - Commissioning and first operation

LHC beam injection tests

August 2008: the ALICE experiment detected “LHC related particles” during the very first injection tests

SPD was recording data and self-triggering with the Pixel Trigger system



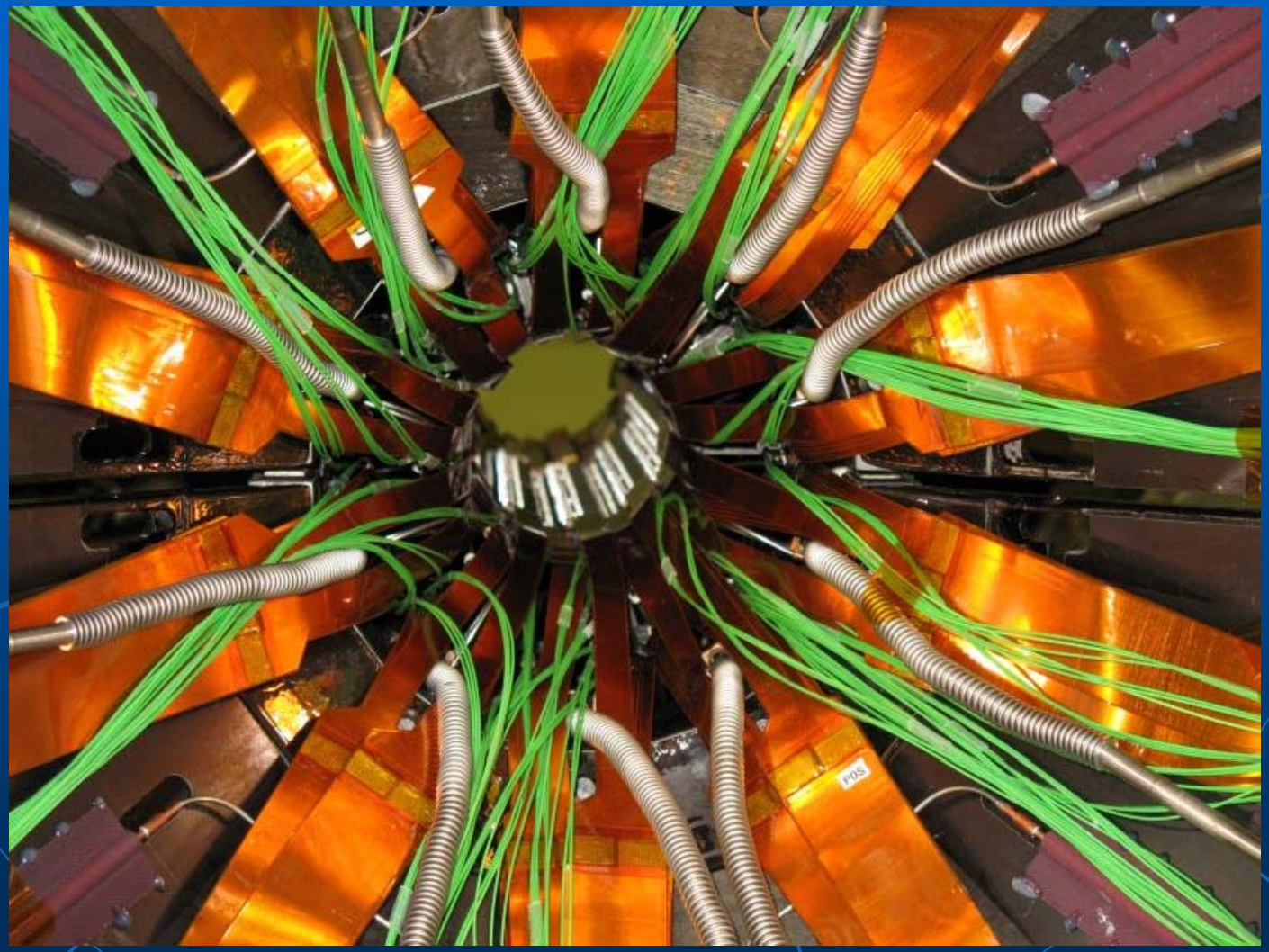
References

References:

- G. Aglieri Rinella et al., "*The Level 0 Pixel Trigger system for the ALICE experiment*", Journal of Instrumentation JINST 2P01007 and Proceedings of the 12th Workshop on Electronics for LHC and Future Experiments, LECC06, September 2006, Valencia, Spain
- A. Kluge et al., "*The ALICE Silicon Pixel Detector*", Nuclear Instruments and Methods A, Volume 582, Issue 3, 1 December 2007, Pages 728-732
- ALICE collaboration, "ALICE physics Performance Report", CERN-LHCC-2003-049, J. Phys., G30 (2004) 1517-1763
- J. Conrad et al., "Minimum Bias Triggers in Proton-Proton collisions with the VZERO and Silicon Pixel Detectors", ALICE Internal note, ALICE-INT-2005-025, 19/10/2005

Spare slides

SPD detector



Triggering with SPD Fast-OR

- Extract and process Fast-OR signals
- Generate input for the Level 0 (fastest) trigger decision
  - 1200 Fast-OR signals on 120 optical links every 100 ns

- Proton-proton
  - *Minimum bias*
  - *High multiplicity studies*
  - Topological selection (jets)
- Heavy ions
  - Selection of impact parameter

- Algorithms
  - Topology (Global OR, Vertex)
  - Multiplicity
  - Boolean functions of 1200 Fast-OR bits

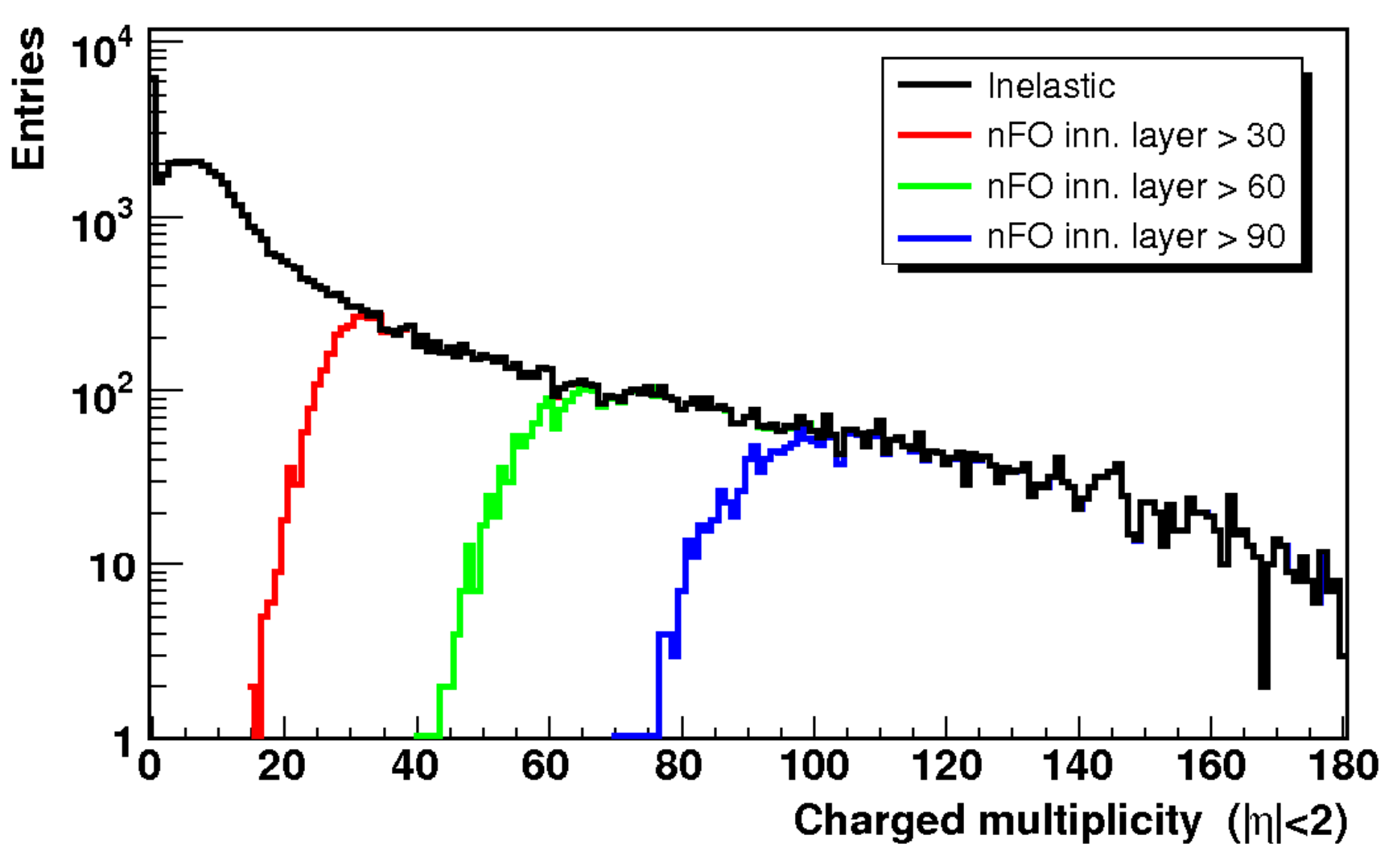
Trigger algorithms

- Combinational (boolean AND/OR) functions of 1200 Fast-OR bits
  - Occupancy (multiplicity)
  - Coincidence trigger (topology)
- Not possible: iterative algorithms on data set

Example: vertex trigger

- Pseudo-Tracklet: one chip hit on inner and one on outer layer, in line with region +/-10 cm around vertex
- Chip map for pixel trigger electronics calculated from simulation: (L11,L21), (L12, L22), … , (L1n, L2n)
- FPGA *looks for at least 1 out of 11000* pseudo-tracklets
  - Processing time 12.4 ns (Xilinx ISE)
  - 4% of FPGA resources (Xilinx ISE)
- FPGA *counts* how many out of 11000 tracklets are present
  - ~27 ns processing time (Xilinx ISE)
  - 5% of FPGA resources (Xilinx ISE)

Multiplicity trigger

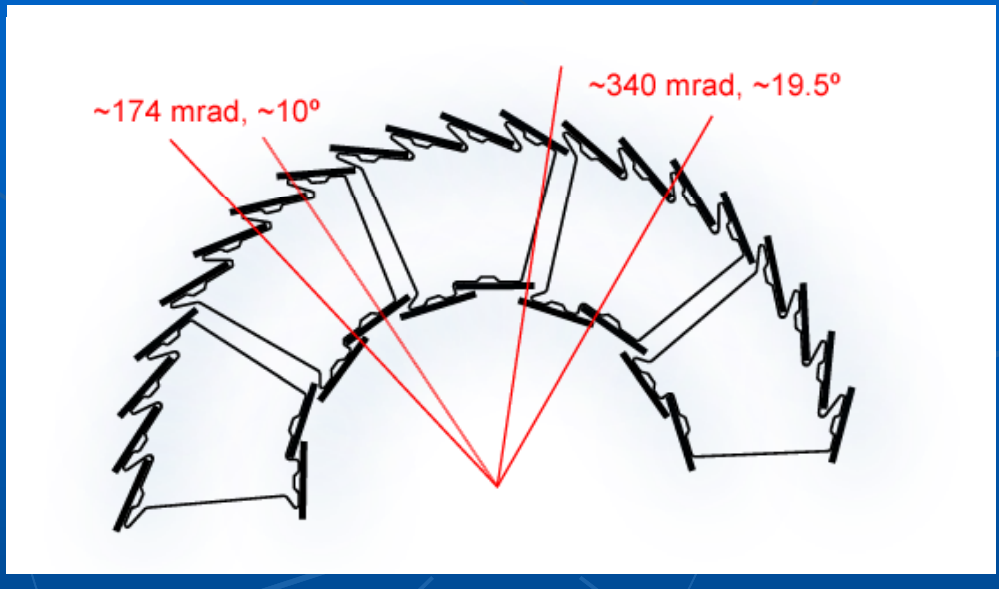


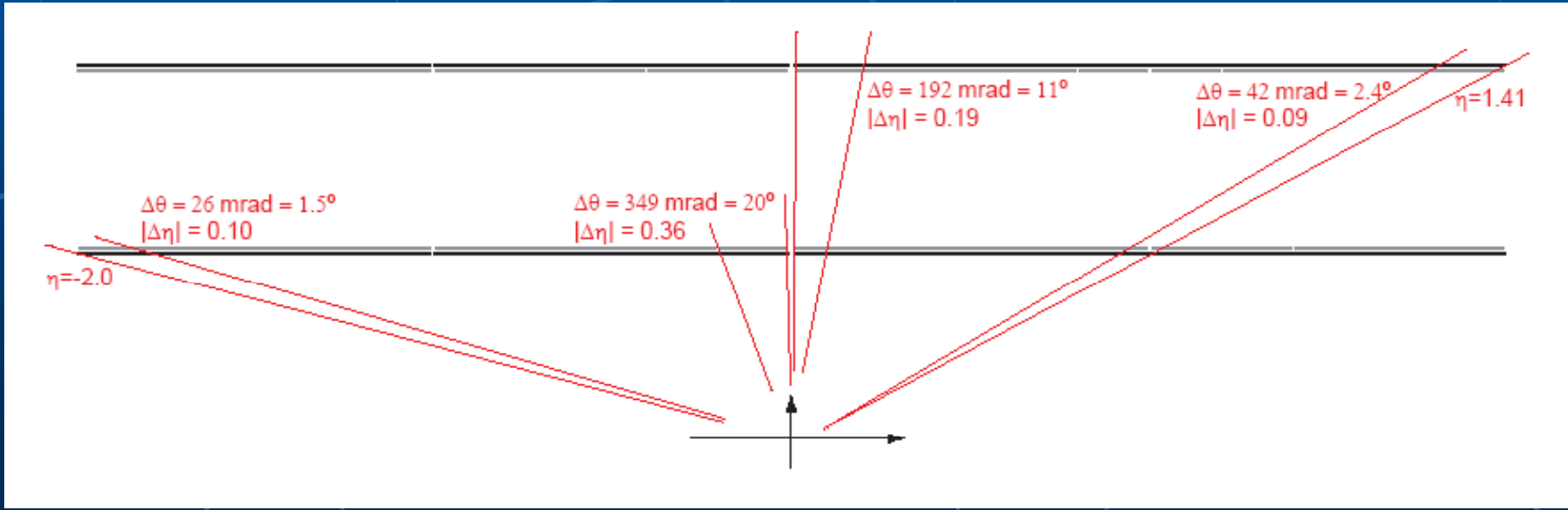
Domenico Elia

ALICE trigger parameters

	Level 0	Level 1	Level 2
Last trigger input at CTP (μs)	0.8	6.1	87.6
Trigger output at CTP (μs)	0.9	6.2	87.7
Trigger input at detectors (μs)	1.2	6.5	
Rate (Hz)		1000	40-800

Angular resolution





Radiation effects

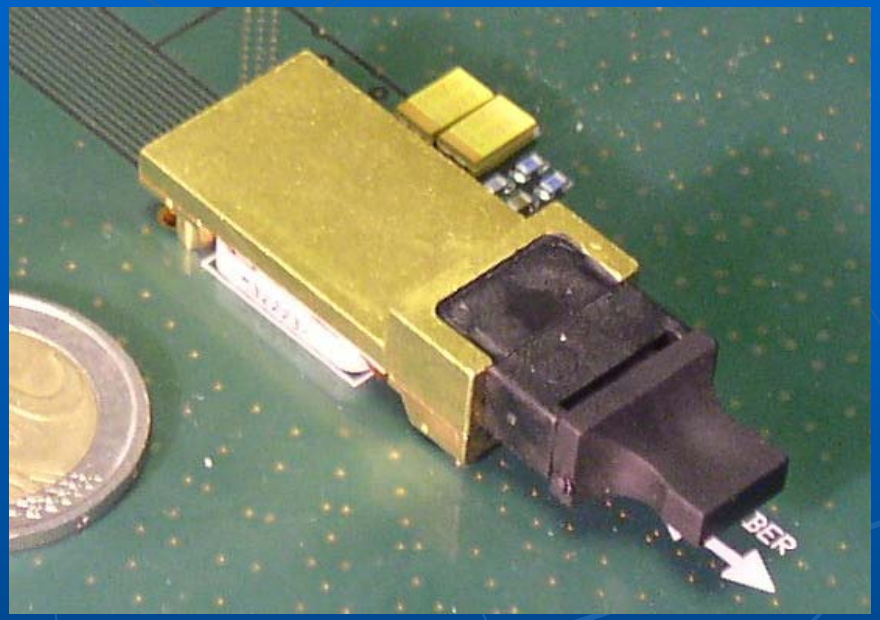
- Radiation Results of the SER Test of Actel, Xilinx and Altera FPGA instances, iROC report, 2004

FIT	SEFI	SEU
Altera EP1C20	453	
Xilinx XC3S1000	320	1240
Xilinx XC2V3000	1150	8680

- Failure In Time (FIT) := errors in 109 hours with neutron flux of 14 $cm^{-2}hr^{-1}$
  - SEFI: Single Event Functional Interrupt
  - SEU: Single Event Upset (configuration)
- Neutron max fluence: 2.0 • 108 cm-2 (10 y)
  - Morsch, Pastircak, Radiation in ALICE Detectors and Electronic Racks, ALICE-INT-2002-28
- Central Trigger Processor using SRAM based ALTERA Cyclone EP1C20

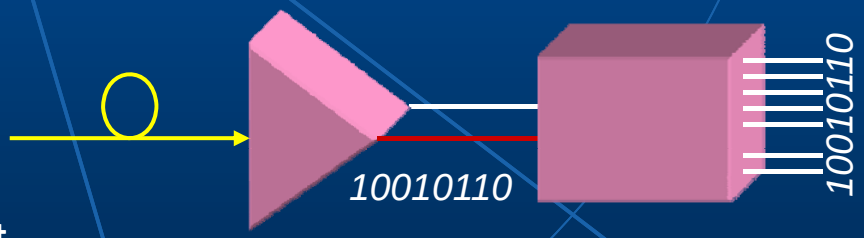
Errors in 10 years	SEFI	SEU
Altera EP1C20	7	
Xilinx XC3S1000	5	18
Xilinx XC2V3000	17	124

Developments



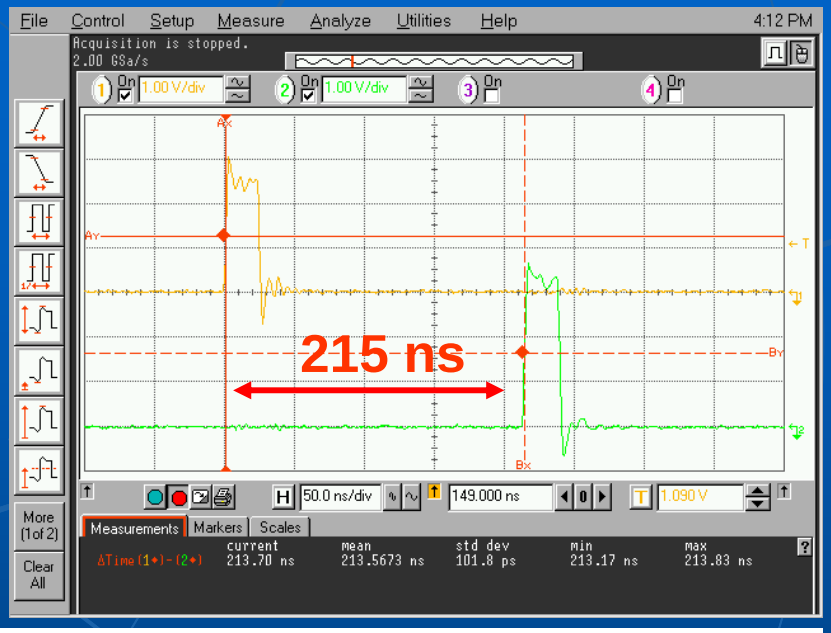
- Advanced 12-channel parallel optical fiber receiver modules
  - Devices customized by Zarlink
    - 1310 nm, single mode
  - Experimentally validated
  - Space saving

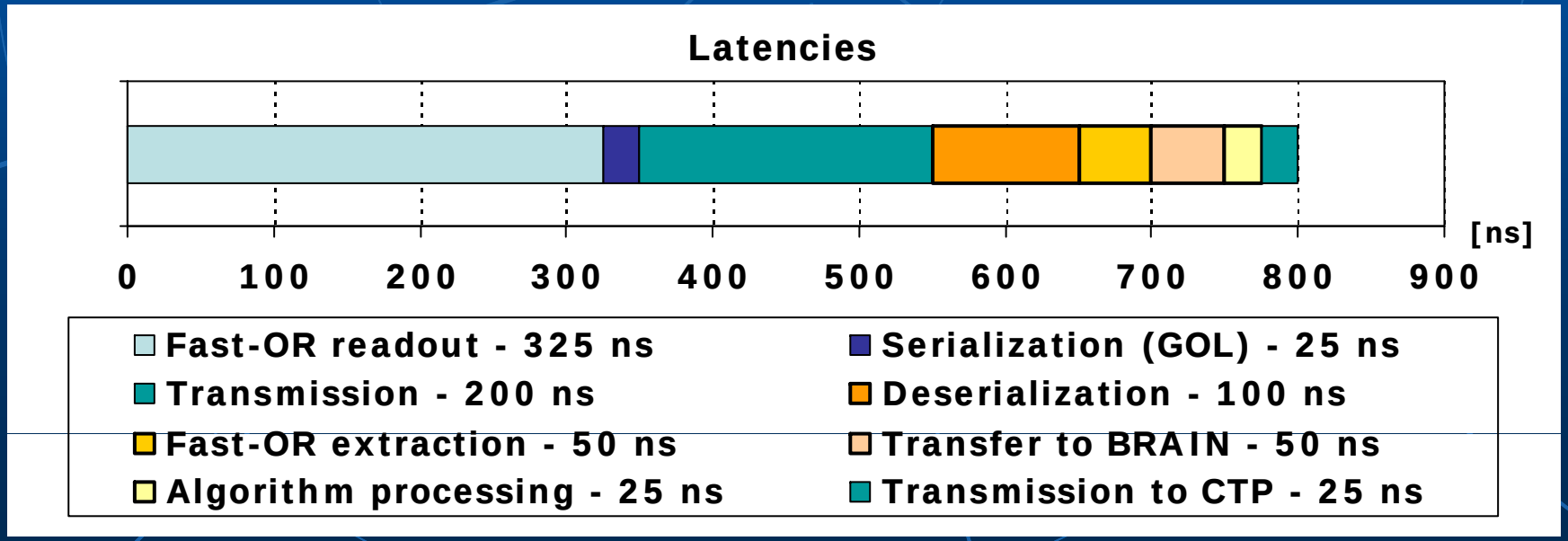
- G-Link protocol deserializers on programmable hardware
  - Implemented and tested with advanced FPGAs
  - Not fulfilling latency requirement
- Dedicated deserializer ASIC



Latencies of processes

- Serialization, deserialization, processing latency
- Hardware emulator of the Silicon Pixel Detector as data source
- Overall latency: 800 ns





Control and configuration

- Status monitoring and control on ALICE DDL communication layer
- User selection of different processing algorithms
  - Download of configuration file into local SRAM memory
  - Reconfiguration of the processing FPGA
- Interfaces to several ALICE subsystems